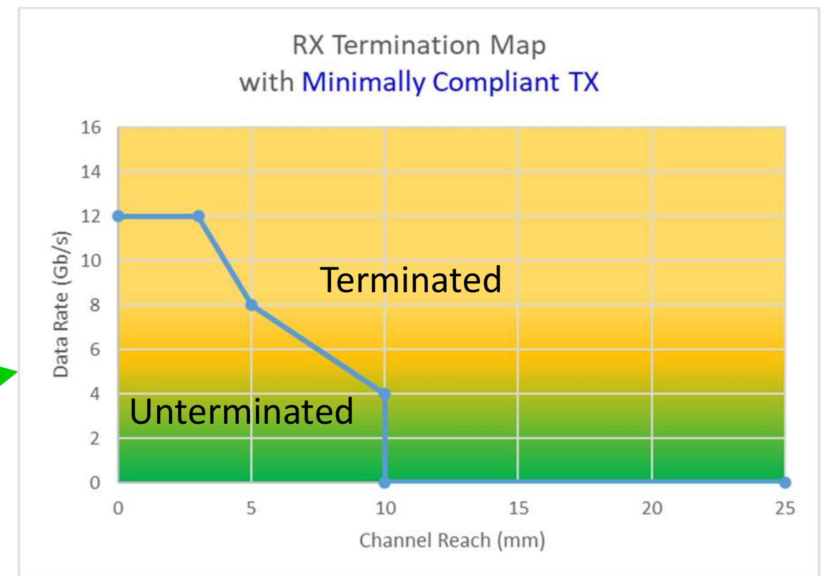
Electrical, Form-Factor, and Compliance

Data Rate, BER, and Channel Reach

- Signaling: Unidirectional NRZ
- Data Rate: 4, 8, 12, 16, 24, 32 Gb/s.
- Channel Reach:
  - Advanced Package (25-55um bump pitch):
    - Up to 2mm and 32Gb/s, TX drive control.
    - No RX Termination
  - Standard Package (100-130um bump pitch):
    - TX Termination
    - RX Termination Map



Reach for unterminated RX can be increased with higher swing TX

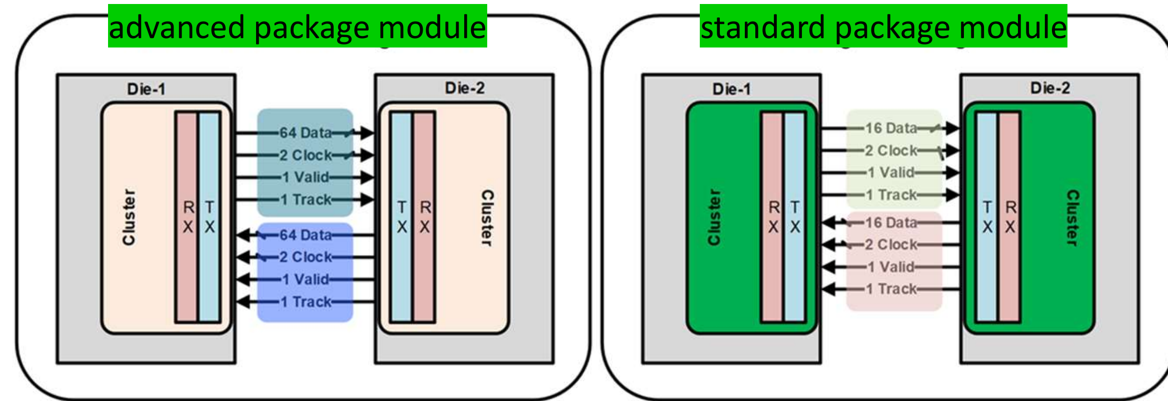
- BER:

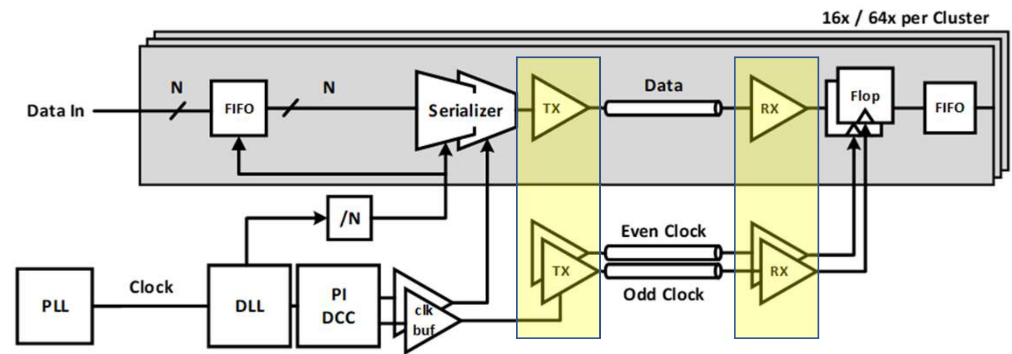
Data Rate (Gb/s)	4	8	12	16	24	32
Advanced Package	1.00E-27	1.00E-27	1.00E-27	1.00E-15	1.00E-15	1.00E-15
Standard Package	1.00E-27	1.00E-27	1.00E-15	1.00E-15	1.00E-15	1.00E-15

CRC and Retry for BER 1E-15 to achieve FIT rate <<1

PHY Architecture

- Basic module data width:
  - x64 for advanced packaging
  - x16 for standard packaging
- Differential Forwarded Clock, Single-Ended Data.
- "Matched" Architecture
  - Better tolerance to power supply noise
- Matched Interconnect Channels
  - Significant power reduction in clock recovery
- SSC allowed, 0 ppm TX to RX





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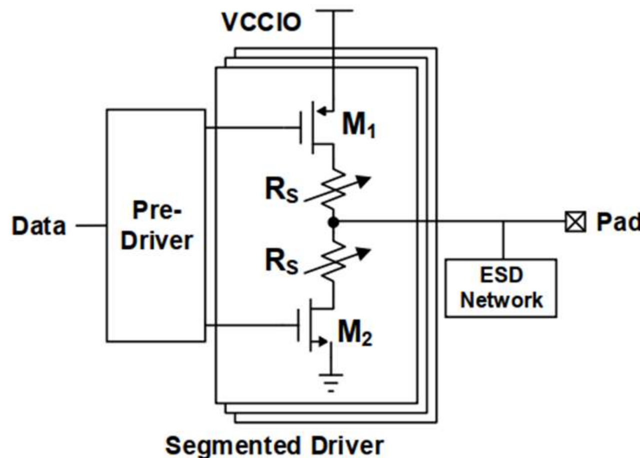
Driver and Input Buffer

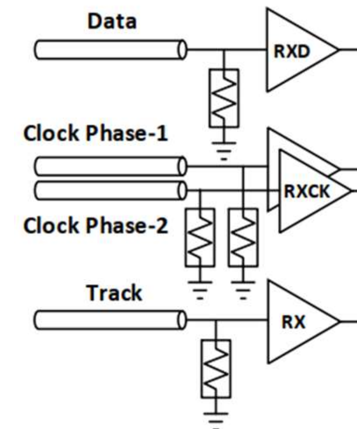
TX Driver

- Typical segmented driver
- CMOS implementation shown. NN driver and other structure possible.
- Target source impedance based on optimal eye open, not necessary matching T-Line impedance.
- BW and rise/fall time defined by Rterm and Cpad spec
- **TXLE** (1-tap de-emphasis) required at 24G+
  - Trained at link-initialization, no realtime adaptation



RX Input Buffer

- Termination (when applicable) is to ground, and matching T-Line impedance.
- Spec does not mandate a specific input buffer design. If RX amplifier is used, recommend BW of > 0.75x data rate (1.5x Nyquist).
- Optional RX CTLE



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TX and RX Voltage Compatibility

- Mininum TX swing 0.4V
- Strongly recommend max TX voltage < 0.85V for compatibility with future process nodes

Transmitter V_{OH} and Receiver VCC compatibility guidelines				
Die 1 TX output maximum V_{OH} (V)	V_{OH}	V_{OH}	V_{OH}	V_{OH}
Die 2 RX AFE VCC level (V)	V_{OH} - VCC < 0mV	V_{OH} - VCC = 0mV	V_{OH} - VCC < 100mV	V_{OH} - VCC > 100mV
Compatibility	Safe	Safe	Safe	Not Safe*

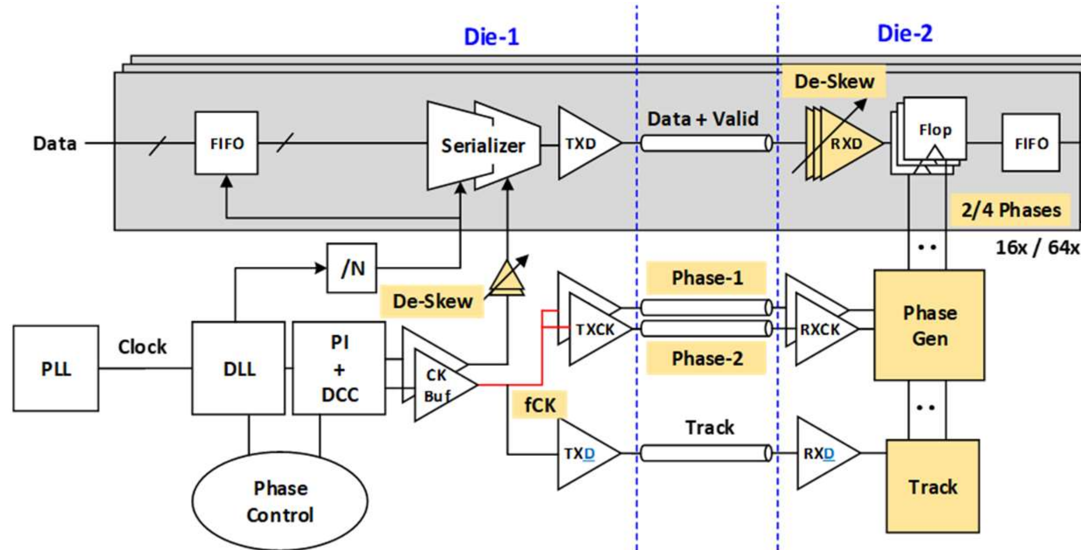
- Cross Process Reliability and Electrical Overstress (EOS) concerns
  - To avoid reliability issues (voltage overstress above allowable process limits: EOS), recommend limiting the TX output high (V_{OH}) to a maximum of 100mV above the RX supply rail.
  - When the TX V_{OH} is equal to or lower than the RX AFE supply rail, within ranges in the spec, there won't be reliability concerns.

- In the case of "Not Safe*", RX AFE overstress protection circuitry can be used to mitigate the issue, at cost of area and power consumption.

PHY Clocking Architecture

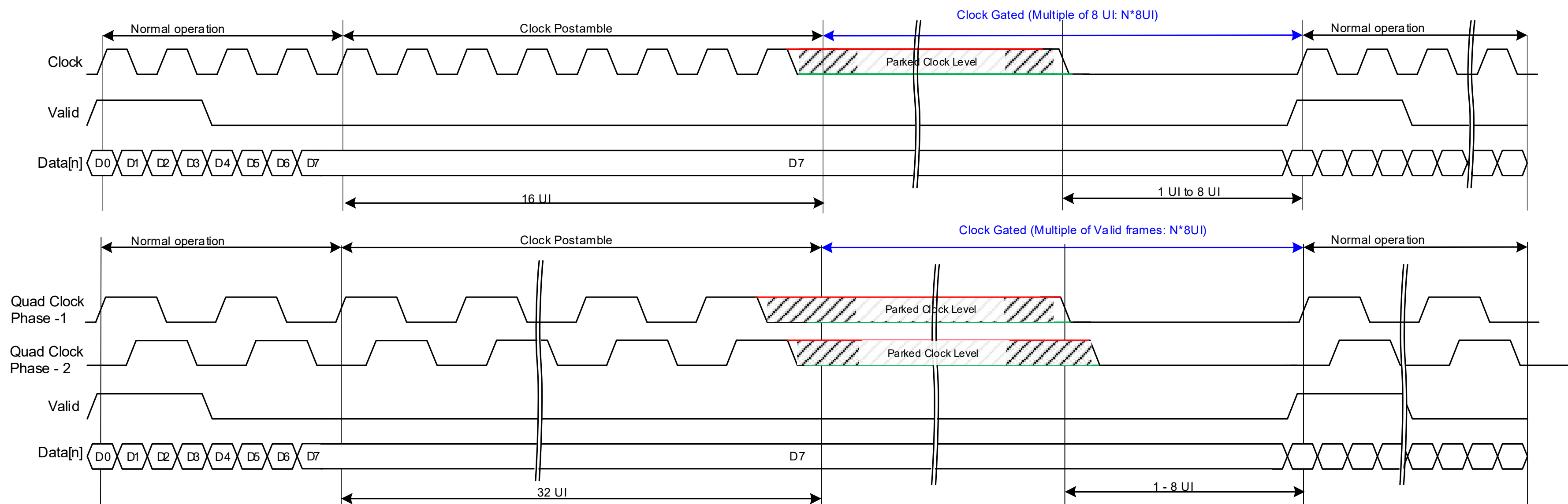
- Supports 2-way and 4-way interleaving TRX
- Independent even/odd phase control
- Global TX, local TX, local RX phase adjustments depending on data rate.
- Data Valid bit to gate clock distribution (also for data framing)
- Track bit for background training and phase alignment

Data rate (GT/s)	Clock freq. (fCK) (GHz)	Phase -1	Phase-2	De-skew (Req/Opt)
32	16	90	270	Required
	8	45	135	Required
24	12	90	270	Required
	6	45	135	Required
16	8	90	270	Required
12	6	90	270	Required
8	4	90	270	Optional
4	2	90	270	Optional



Dynamic Clock Gating

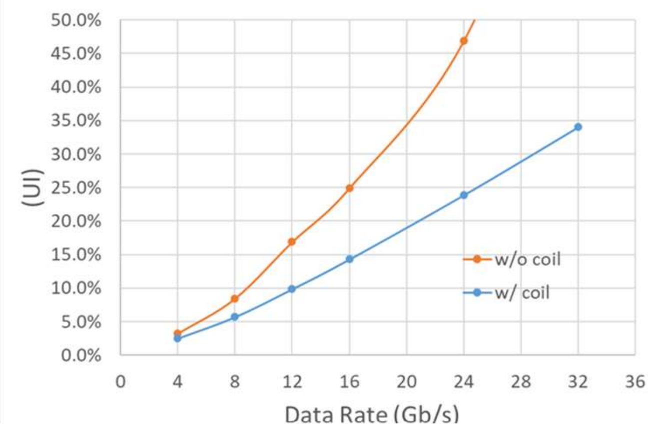
- Clock gated if Valid remains low after providing postamble
  - No clock gating if free running clock mode is negotiated
- Clock parked Hi/Low during alternate clock gating events; 8 UI boundary

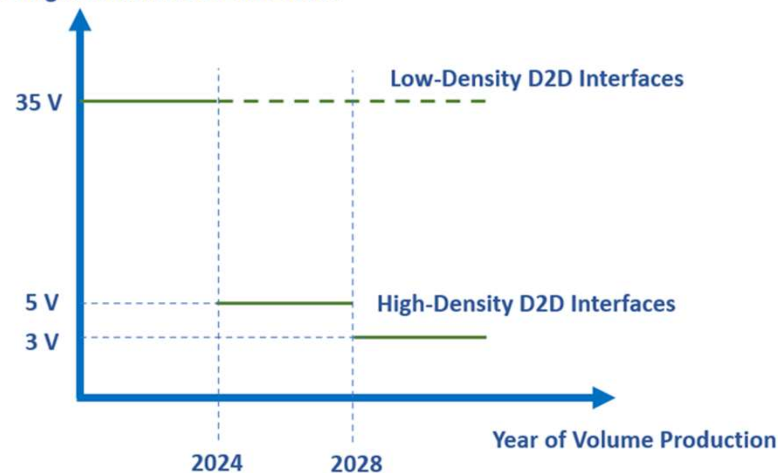


Pad Capacitance and ESD

- Cpad has 1st order performance impact
- Aggressive targets on Cpad and ESD
- UCIe 1.0 ESD spec: **30V CDM,** further scaling in future, align with Industry Council on ESD Targets.
- **T-coil** to reduce effective pad capacitance
  - T-coil widely used by serial I/O across industry
  - T-coil size expected to be on the order of 20um x 20um x2

TX/RX Pad Capacitance	250/200	fF	Advanced Package Mode
TX/RX Pad Capacitance (8Gb/s capable design)	300	fF	Standard Package Mode
TX/RX Pad Capacitance (16Gb/s capable design)	200	fF	Standard Package Mode Effective Cpad
TX/RX Pad Capacitance (32Gb/s capable design)	125	fF	Standard Package Mode Effective Cpad





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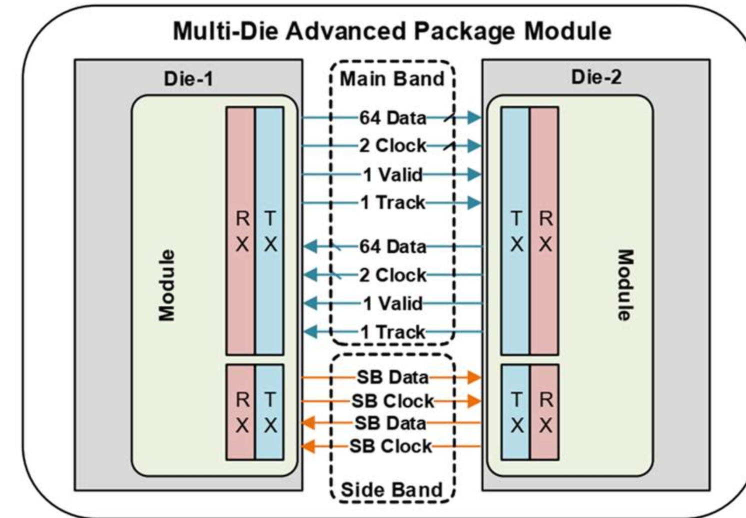
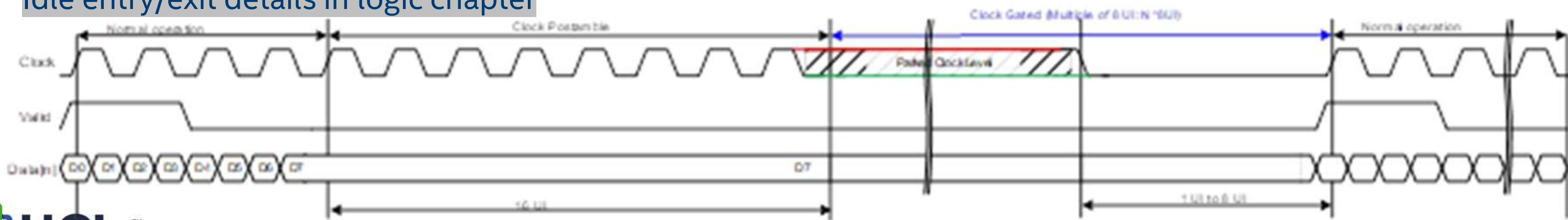
Other PHY Features

- 800MT/s 2-wire sideband per module
- Global signals (DFX etc.)
- Low Datapath Latency: 12 UI up to 16Gb/s, 16 UI 24-32Gb/s.
- Ultra Fast Idle Exit:
    - L0-idle Power State through Data Valid Clock gating
- L1 power state (options for further power down)
- Redundancy & Repair for Advanced Package
    - Two per 32 bits
- Data Scrambling to mitigate power supply noise



Sideband used for training, debug, management…
Figure is logical illustration
Physically sideband leverages depopulated bumps
No impact to shoreline / die edge BW density

Idle entry/exit details in logic chapter



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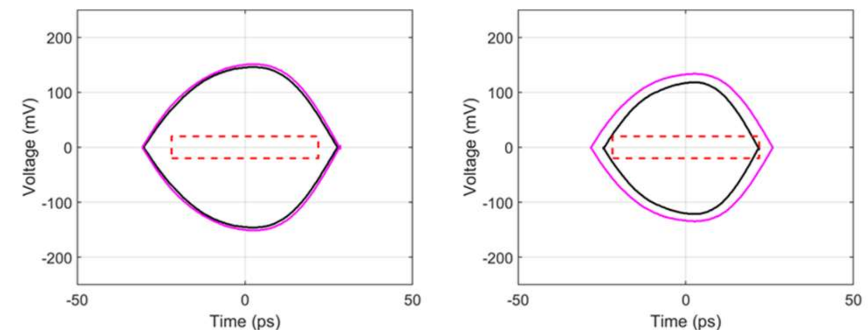
Channel Specification

- Channel needs to meet minimum eye mask under channel compliance simulation with noiseless jitter-less behavioral TX and RX models

Data Rate	4-16Gb/s	24-32Gb/s
Overall (Eye Closure due to Channel)		
Eye Height	40mV	40mV
Eye Width (rectangular eye mask with specified eye height)	0.75 UI	0.65 UI with Equalization Enabled

Pass/fail eye mask example



Insertion loss and Crosstalk spec defined based on the criteria using Voltage Transfer Function (VTF) method

- Due to short transmission line, VTF is more practical than S-parameter based method.

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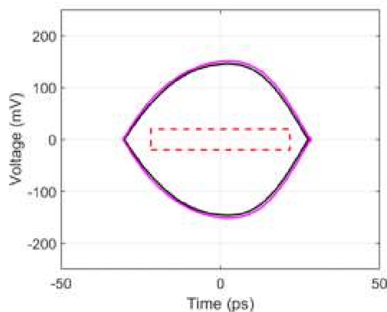
Tightly Coupled Mode

- Both Conditions must be met:
  - Shared Power Supply or Forwarded Power Supply
  - Channel supports larger eye mask
- Rationale / Advantages:
  - Further Optimization of PHY Circuits to lower power. For example, inverter-based RX, no front amplifier.
  - Reduced Training Complexity, such RX reference voltage training.
  - Preparation for higher density D2D



Data Rate	4-16Gb/s	24-32Gb/s
Overall (Eye Closure due to Channel)		
Eye Height	40mV	40mV
Eye Width (rectangular eye mask with specified eye height)	0.75 UI	0.65 UI with Equalization Enabled

Eye mask for channel changes to

250mV / 0.7UI for TX swing 0.75V

Up to 16Gb/s

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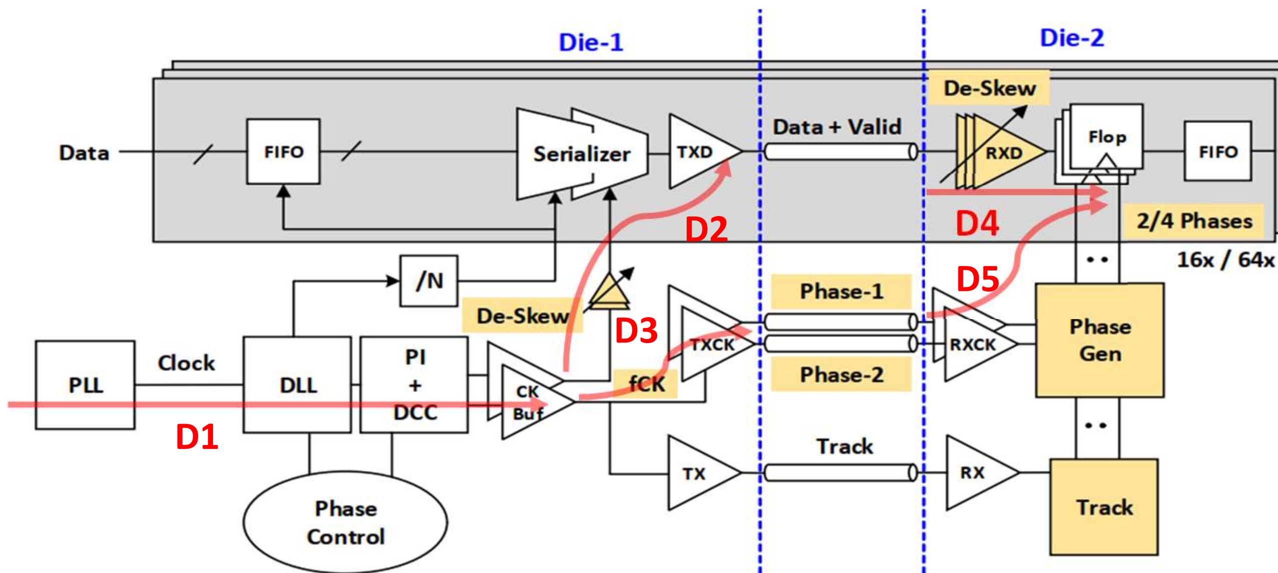
TX and RX Jitters

Specify 1-UI TX jitter, data/clock differential TX jitter, and data/clock differential RX jitter.



D1: Tx Common clock delay
D2: Tx Data path clock delay
D3: Tx FWD clock path delay
D4: Rx Data path delay
D5: Rx Clock path delay

E(D3) = E(D2) + nT, E is the mean, n = 0.5 for matched arch

Jitter = D1(t-nT) – D1(t) + D3(t-nT) – D2(t) – nT + D5(t) – D4(t)

➔ Jitter = D(t-nT) – D(t) + $\delta D_T(t)$ – nT + $\delta D_R(t)$

where D = D1+D3 (total delay), δD_T = D3-D2 , $\delta D_R(t)$ = D5-D4

Link Timing Analysis

Timing parameters

	Name	Note
Eye Closure due to Channel	Ch	from SI analysis
Channel Mismatch	Chm	
n-UI TX Total Jitter	Tjnui	specified at BER
TX Data/Clock Differential Jitter	Tjtx	specified at BER
TX Duty Cycle Error	Dce	post correction
TX Lane-to-lane Skew Correction Range	Rstx	
TX Lane-to-Lane Skew	Stx	post correction
Clock to Mean Data Training Accuracy	Eckd	including static and tracking error
RX Data/Clock Differential Jitter	Tjrx	specified at BER
Max RX Lane-to-Lane Skew	Msrx	if exceeding limit, requires RX lane-to-lane deskew
RX Phase Error	Eph	including duty cycle and I/Q mismatch
Sampling Aperture	Ap	

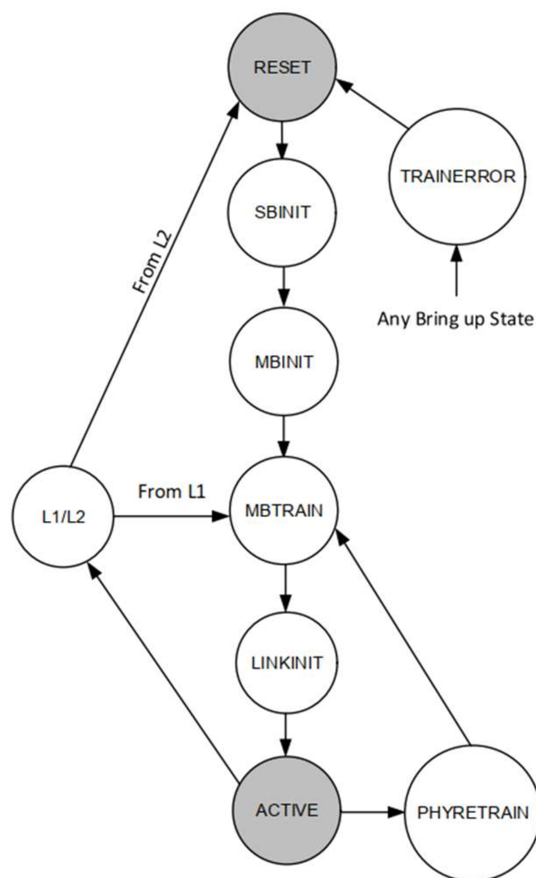
- Need to meet the following conditions (range defined as peak-to-peak)

$$C_h + T_{jnui} + D_{ce} + S_{tx} + E_{ckd} + T_{jrx} + E_{ph} + A_p \leq 1\text{UI}$$

$$C_{hm} \leq R_{stx} - M_{srx}$$

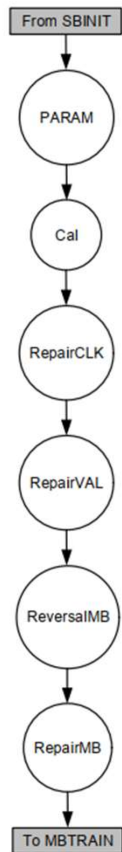
- Detailed numbers at different data rates are in the spec and WG discussions

Link Training and Status State Machine



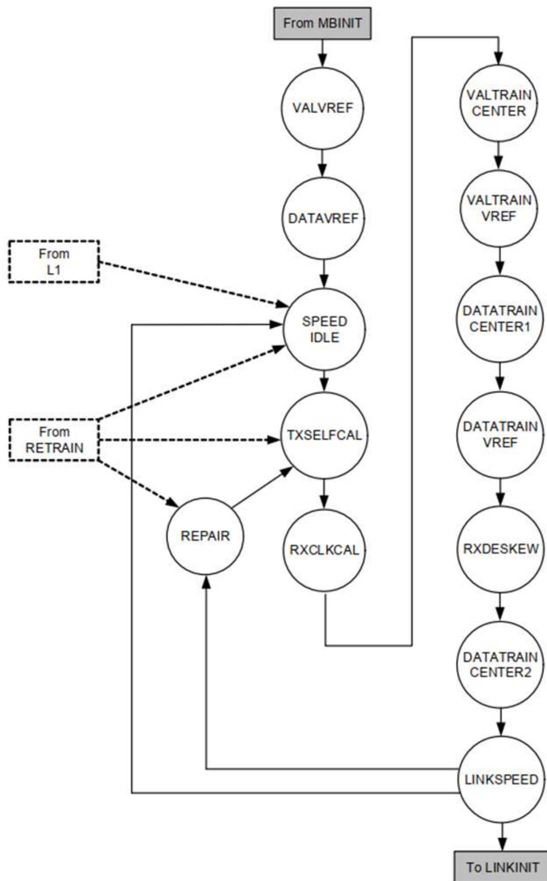
- Sideband (SB) initialization
  - Initialization and repair (advanced interface) of SB
- Main band (MB) initialization
  - Parameter exchange, CLK, Valid & MB repair & MB reversal
- Main band training
  - Data training, at speed repair/degrade and speed degrade
- Link init
  - Exchange RDI Link management messages
- PHYRETRAIN: Retrain based on Link errors
  - Allow infield repair and degrade
- L1/L2: Lower power state
- Train error: For uncorrectable internal errors and Link down conditions //state timeouts and SB timeouts
- Active: Transactions are sent and received

Main band Initialization



- Data rate set to 4GT/s for main band
- Param
  - Exchange of parameters required to setup maximum speed and other PHY settings
- Cal
  - Perform any required calibration (ex: Tx Duty Cycle, Rx Vref etc.)
- RepairCLK
  - Detect and apply repair (if needed) to clock and track Lanes for Advanced Pkg
  - Functional check of clock and track Lanes for Standard Pkg
- RepairVAL
  - Detect and apply repair (if needed) to Valid Lane for Advanced Pkg
  - Functional check of Valid for Standard Package interface.
- ReversalMB
  - Detect and apply Lane reversal (both Standard and Advanced package)
- RepairMB
  - Detect and apply repair (if needed) for Advanced Pkg interface
  - Functional check and width degrade (if needed) for Standard Pkg interface.

Main band Training



- VALVREF
  - Receiver reference voltage (Vref) to sample the incoming Valid
  - Performed through Rx initiated point tests or sweep using Valtrain pattern
- DataVref
  - Receiver reference voltage (Vref) to sample the incoming Data
  - Performed through Rx initiated point tests or sweep using LFSR pattern
- Speed Idle
  - Frequency changed to highest negotiated Data rate
- TxSelfCal
  - UCIe Module calibrates its circuit parameters independent of the UCIe Module Partner
- RxClkCal
  - Perform calibration on Clock receive path and align Clock/Track alignment
- ValTrainCenter
  - Valid to clock centering and ensure Valid functionality

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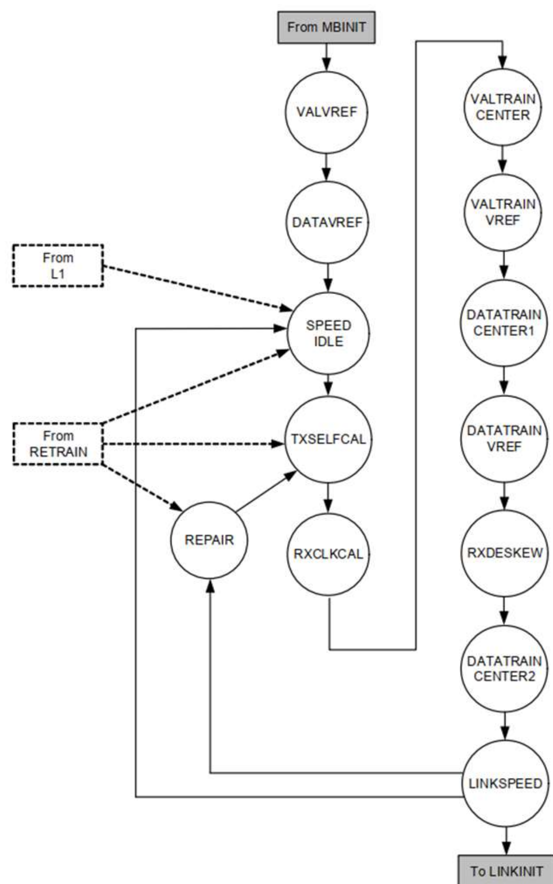
Main band Training [2]



- ValTrainVref
  - Optional operation within the state to allow at speed Vref training on Valid signal
- DataCenter1
  - Full Data to clock training with correct Valid framing
  - Tx initiated point tests or eye width sweep with LFSR pattern
- DataTrainVref
  - Optional operation within the state to allow at speed Vref training on Data
- RxDeSkew
  - Optional Operation within the state to allow Lane-to-Lane skew correction on Rx if needed
- DataCenter2
  - Recentering if Rx performs Deskew
- LinkSpeed
  - Link stability check; direct Link to repair or speed degrade if needed
- Repair
  - Apply repair for Advanced pkg and Width degrade for Standard pkg

Electrical Summary

	Standard Package	Standard Package	Standard Package	Standard Package	Advanced Package	Advanced Package	Advanced Package
Data Width	16	16	16	16	64	64	64
Data Rate (Gb/s)	4-16	4/8/12	16	24/32	4/8/12	16	24/32
Power Efficiency Target (pJ/b)	0.25-0.5	0.5-1	0.5-1	0.75-1.25	0.25-0.5	0.3-0.6	0.3-0.6
Latency Target (TX+RX) (UI)	12	12	12	16	12	12	16
Idle Power (% of peak)	15%	15%	15%	15%	15%	15%	15%
Channel Reach (mm)	2-10	25	25	25	2	2	2
Die Edge BW Density (GByte/s/mm)	28-112	28-84	112	168/224	165-494	658	988/1317
BW Area Density (GByte/s/mm²)	21-85	21/42/64	85	109/145	158/316/473	631	710/947
PHY dimension Width (um)	571.5	571.5	571.5	571.5	388.8	388.8	388.8
PHY dimension Depth (um)	1320	1320	1320	1540	1043	1043	
ESD	**30V CDM (Further scaling in future, align with Industry Council on ESD Targets)**						

Advanced package PHY depth depends on bump pitch, number based on 45um

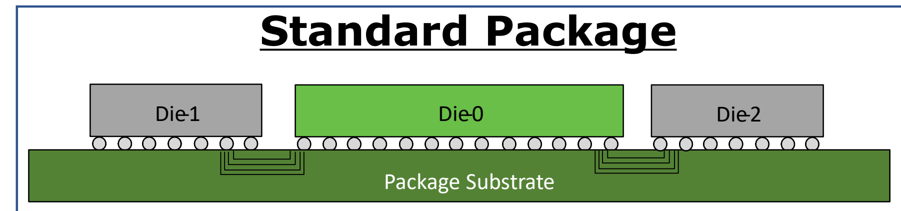
Coffee Break

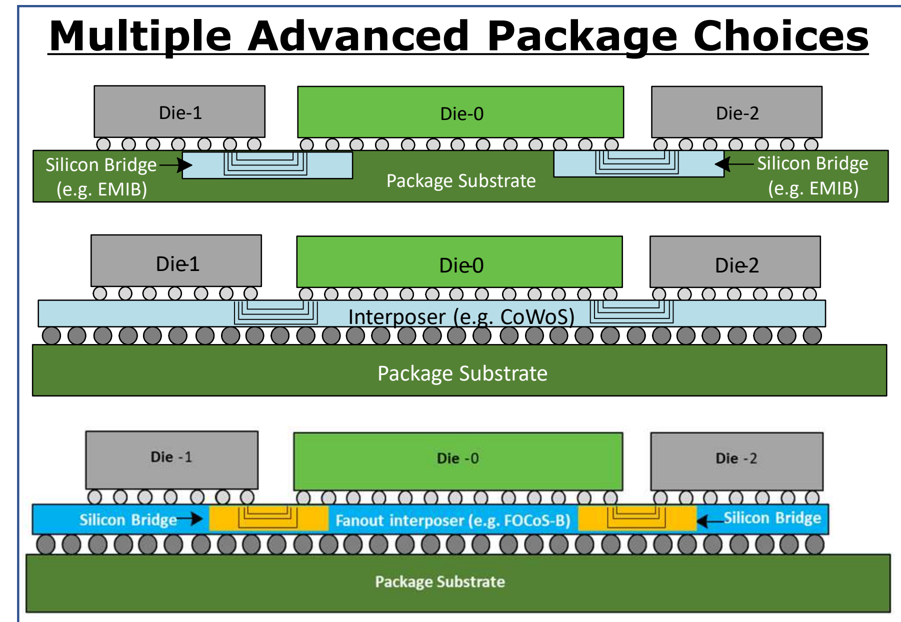
UCIe 1.0: Supports Standard and Advanced Packages

- Standard Package: 2D – cost effective, longer distance
- Advanced Package: 2.5D – power-efficient, high bandwidth density
- Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE
Data Rate (GT/s)	4, 8, 12, 16, 24, 32	
Width (each cluster)	16	64
Bump Pitch (um)	100 – 130	25 - 55
Channel Reach (mm)	<= 25	<=2

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317
B/W Density (GB/s/mm^2)	22-125	188-1350





UCIe 1.0 spec supports multiple packaging technology options to build an open ecosystem

UCIe-S: Standard Package Bump Maps

- Two options: x16 and x32 bump arrangements for BW/mm flexibility
  - 4-2-4 recommended package stack-up for x16 (two topside stripline routing layers)
  - 8-2-8 recommended package stack-up for x32 (4 topside stripline routing layers) for doubled BW/mm

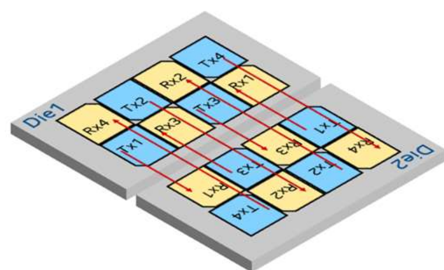
x16 module

Column 0	Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8	Column 9	Column 10	Column 11
	txdatasb		txcksb		vccaon		vccaon		rxcksb		rxdatasb
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vss		vss		vss		vss
vccio		txdata7		txdata9		vccio		rxdata8		rxdata6	
	txdata5		txckn		txdata11		rxdata10		rxckp		rxdata4
vss		vss		vss		vss		vss		vss	
	txdata4		txckp		txdata10		rxdata11		rxckn		rxdata5
vss		txdata6		txdata8		vss		rxdata9		rxdata7	
	vss		vss		vss		vss		vss		vss
vccio		txdata3		txdata13		vccio		rxdata12		rxdata2	
	txdata1		txvld		txdata15		rxdata14		rxtrk		rxdata0
vccio		vss		vss		vccio		vss		vss	
	txdata0		txtrk		txdata14		rxdata15		rxvld		rxdata1
vss		txdata2		txdata12		vss		rxdata13		rxdata3	
Die Edge											

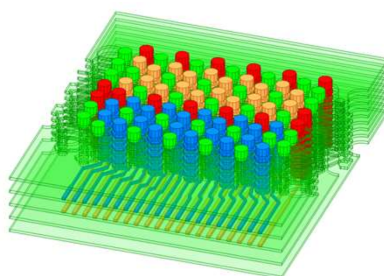
x32 module

Column 0	Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8	Column 9	Column 10	Column 11
	m2rxdatasb		m2rxcksb		vccaon		m2txcksb		m2txdatasb		vccaon
m1txdatasb		m1txcksb		vccaon		vccaon		m1rxcksb		m1rxdatasb	
	vccio		vccio		vccio		vccio		vccio		vccio
vss		vss		vss		vss		vss		vss	
	m2rxdata6		m2rxdata8		vss		m2txdata9		m2txdata7		vss
m2rxdata4		m2rxckp		m2rxdata10		m2txdata11		m2txckn		m2txdata5	
	vss		vss		vss		vss		vss		vss
m2rxdata5		m2rxckn		m2rxdata11		m2txdata10		m2txckp		m2txdata4	
	m2rxdata7		m2rxdata9		vss		m2txdata8		m2txdata6		vss
vss		vss		vss		vss		vss		vss	
	m2rxdata2		m2rxdata12		vss		m2txdata13		m2txdata3		vss
m2rxdata0		m2rxtrk		m2rxdata14		m2txdata15		m2txvld		m2txdata1	
	vss		vss		vss		vss		vss		vss
m2rxdata1		m2rxvld		m2rxdata15		m2txdata14		m2txtrk		m2txdata0	
	m2rxdata3		m2rxdata13		vccio		m2txdata12		m2txdata2		vccio
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vccio		vss		vss		vccio
vccio		m1txdata7		m1txdata9		vccio		m1rxdata8		m1rxdata6	
	m1txdata5		m1txckn		m1txdata11		m1rxdata10		m1rxckp		m1rxdata4
vss		vss		vss		vss		vss		vss	
	m1txdata4		m1txckp		m1txdata10		m1rxdata11		m1rxckn		m1rxdata5
vss		m1txdata6		m1txdata8		vss		m1rxdata9		m1rxdata7	
	vss		vss		vss		vss		vss		vss
vccio		m1txdata3		m1txdata13		vccio		m1rxdata12		m1rxdata2	
	m1txdata1		m1txvld		m1txdata15		m1rxdata14		m1rxtrk		m1rxdata0
vccio		vss		vss		vccio		vss		vss	
	m1txdata0		m1txtrk		m1txdata14		m1rxdata15		m1rxvld		m1rxdata1
vss		m1txdata2		m1txdata12		vss		m1rxdata13		m1rxdata3	
Die Edge											

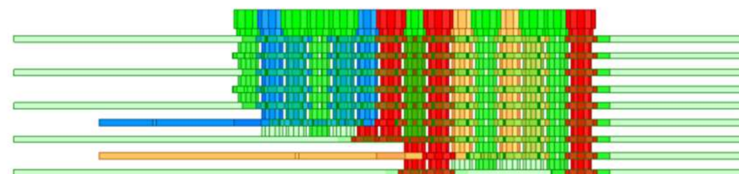
UCIe-S: Arrangement & Channel Characteristics



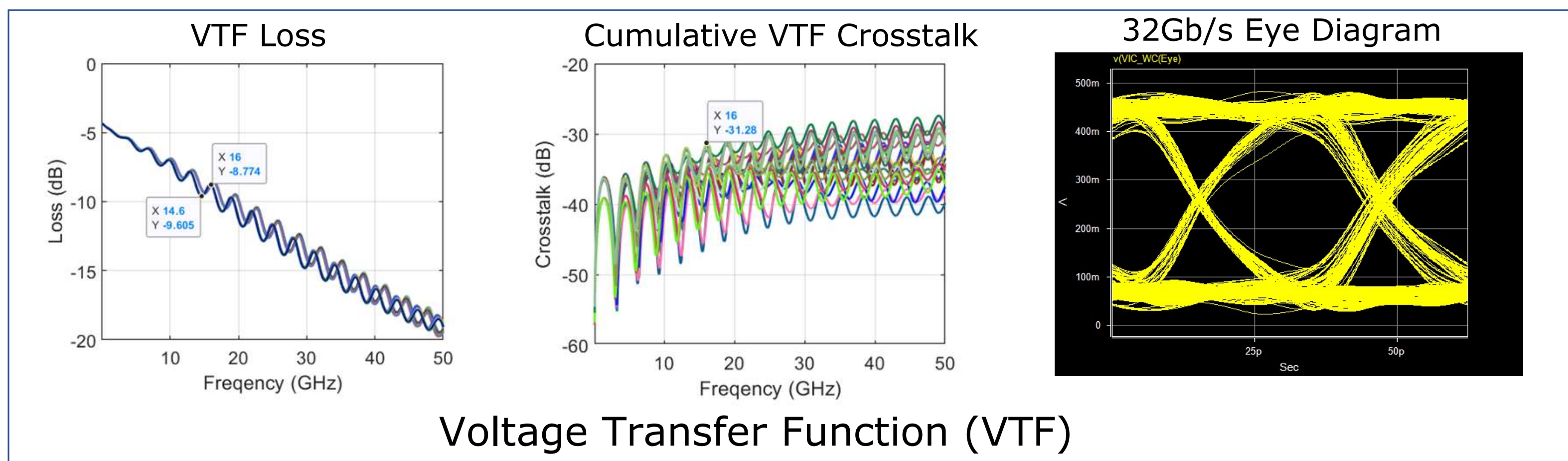
- 2-module stacking



- 18 IO/mm/layer
- 2 routing layers for each module
- 4 routing layers for 2 modules



- power
- ground
- signals on L8
- signals on L6
- signals on L4 and L2 not shown



Voltage Transfer Function (VTF)

25mm length

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2023

UCIe-A Bump Maps

- Bumpout configurations for maintaining optimized BW/mm^2 across allowable bump pitch range
  - 8, 10 and 16-columns
  - Suggested usage guideline:

BP	Max Data Rate by Spec	Columns within 388.8 shoreline
25-30	12	16
31-37	16	
38-44	24	10
45-50	32	
51-55	32	8

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
30		vss		vss		vccio		vccio		vccio		vccio		vss		vss
29	vss		vss		vccio		vccio		vccio		vccio		vss		vss	
28		vss		rxcksbRD		rxcksb		vss		rxdatasb		rxdatasbRD		vss		vss
27	vss		txdatasbRD		txdatasb		vss		vss		txcksb		txcksbRD		vss	
26		rxdata54		rxdata50		rxdata35		vss		rxdata29		rxdata14		rxdata11		rxdataRD0
25	vss		rxdata52		rxdata49		rxdata34		rxdataRD1		rxdata28		rxdata13		rxdata9	
24		rxdata55		rxdata51		rxdata36		rxdataRD2		rxdata30		rxdata15		rxdata10		vss
23	rxdataRD3		rxdata53		rxdata48		rxdata33		vss		rxdata27		rxdata12		rxdata8	
22		rxdata61		vss		rxdata37		vss		rxdata31		rxdata16		vss		rxdata0
21	rxdata63		rxdata56		rxdata47		rxdata32		rxckRD		rxdata26		rxdata17		rxdata2	
20		rxdata60		rxdata46		vss		rxvldRD		rxdata25		vss		rxdata7		vss
19	vss		rxdata57		rxdata43		rxdata38		rxckn		rxdata23		rxdata18		rxdata3	
18		rxdata59		rxdata45		rxdata40		rxvld		vss		rxdata20		rxdata6		rxdata1
17	rxdata62		rxdata58		rxdata42		rxdata39		rxckp		rxdata22		rxdata19		rxdata4	
16		vss		rxdata44		rxdata41		rxtrk		rxdata24		rxdata21		rxdata5		vss
15	vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio	
14		vccio		vccio		vccio		vccio		vccio		vccio		vccio		vccio
13	vss		txdata5		txdata21		txdata24		txtrk		txdata41		txdata44		vss	
12		txdata4		txdata19		txdata22		txckp		txdata39		txdata42		txdata58		txdata62
11	txdata1		txdata6		txdata20		vss		txvld		txdata40		txdata45		txdata59	
10		txdata3		txdata18		txdata23		txckn		txdata38		txdata43		txdata57		vss
9	vss		txdata7		vss		txdata25		txvldRD		vss		txdata46		txdata60	
8		txdata2		txdata17		txdata26		txckRD		txdata32		txdata47		txdata56		txdata63
7	txdata0		vss		txdata16		txdata31		vss		txdata37		vss		txdata61	
6		txdata8		txdata12		txdata27		vss		txdata33		txdata48		txdata53		txdataRD3
5	vss		txdata10		txdata15		txdata30		txdataRD2		txdata36		txdata51		txdata55	
4		txdata9		txdata13		txdata28		txdataRD1		txdata34		txdata49		txdata52		vss
3	txdataRD0		txdata11		txdata14		txdata29		vss		txdata35		txdata50		txdata54	
2		vccio		vccio		vccio		vccio		vccio		vccio		vccio		vccio
1	vccio		vccio		vccio		vccio		vccio		vccio		vccio		vccio	
	die edge															

16Col
Recommended for
25-37um bump pitch

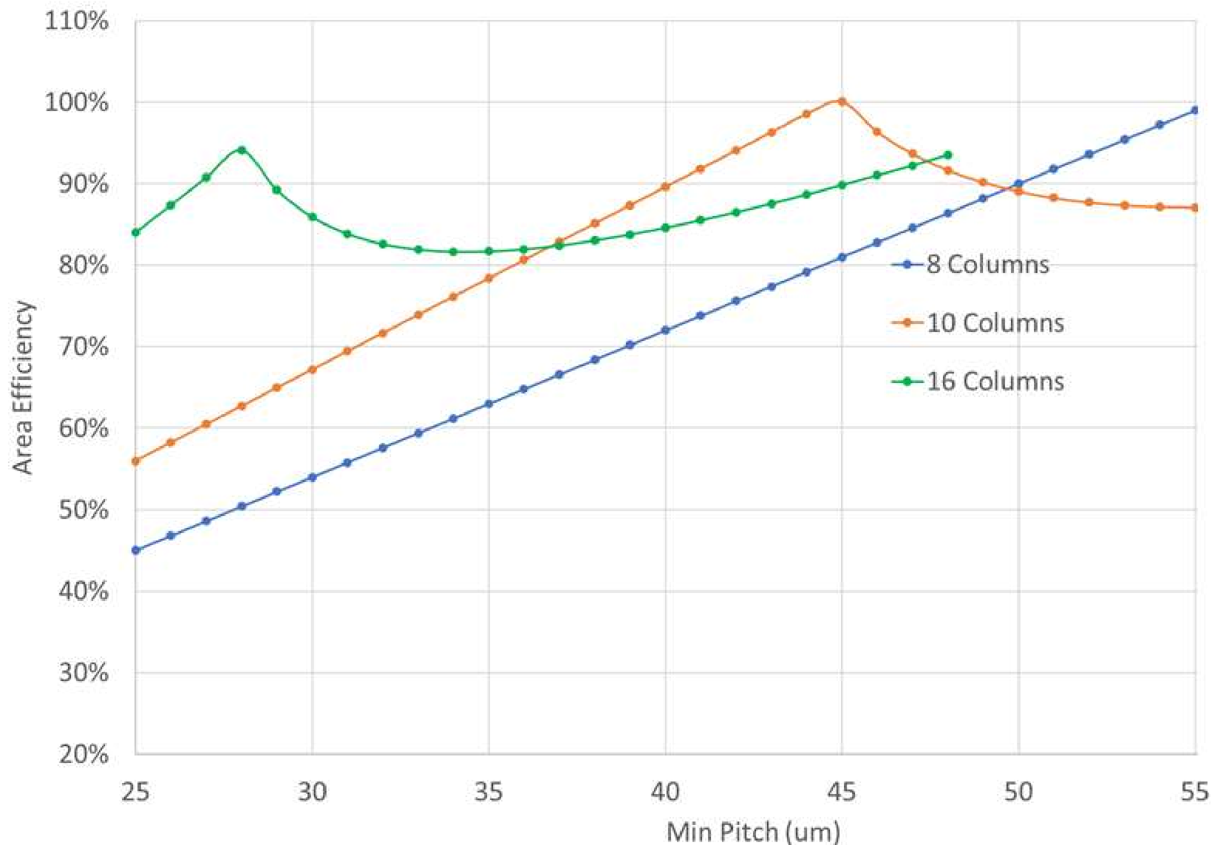
	1	2	3	4	5	6	7	8	9	10
45	vss		vss		vccio		vccio		vss	
44		vss		vccio		vccio		vss		vss
43	vss		vss		vccio		vccio		vss	
42		rxcksbRD		rxcksb		vccio		rxdatasb		rxdatasbRD
41	txdatasbRD		txdatasb		vccio		txcksb		txcksbRD	
40		rxdata50		rxdata35		rxdata29		rxdata14		rxdataRD0
39	rxdataRD3		rxdata49		rxdata34		rxdata28		rxdata13	
38		rxdata51		rxdata36		rxdata30		rxdata15		vss
37	rxdata63		vccio		rxdata33		vccio		rxdata12	
36		rxdata52		vss		rxdata31		vss		rxdata0
35	vss		rxdata48		rxdata32		rxdata27		rxdata11	
34		rxdata53		rxdata37		rxdataRD1		rxdata16		rxdata1
33	rxdata62		rxdata47		rxdataRD2		rxdata26		rxdata10	
32		rxdata54		rxdata38		vss		rxdata17		vss
31	rxdata61		rxdata46		vccio		rxdata25		rxdata9	
30		rxdata55		rxdata39		rxckRD		rxdata18		rxdata2
29	vss		rxdata45		rxvldRD		rxdata24		rxdata8	
28		rxdata56		vss		rxckn		rxdata19		rxdata3
27	rxdata60		rxdata44		rxvld		vss		rxdata7	
26		rxdata57		rxdata40		rxckp		rxdata20		vss
25	rxdata59		rxdata43		rxtrk		rxdata23		rxdata6	
24		rxdata58		rxdata41		vss		rxdata21		rxdata4
23	vss		rxdata42		vccio		rxdata22		rxdata5	
22		vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio
21	vccio		txdata21		vccio		txdata41		txdata58	
20		txdata5		txdata22		vss		txdata42		vss
19	txdata4		txdata20		txckp		txdata40		txdata57	
18		txdata6		txdata23		txtrk		txdata43		txdata59
17	vss		txdata19		txckn		vss		txdata56	
16		txdata7		vss		txvld		txdata44		txdata60
15	txdata3		txdata18		txckRD		txdata39		txdata55	
14		txdata8		txdata24		txvldRD		txdata45		vss
13	txdata2		txdata17		vccio		txdata38		txdata54	
12		txdata9		txdata25		vss		txdata46		txdata61
11	vccio		vccio		vccio		vccio		vccio	
10		txdata10		txdata26		txdataRD2		txdata47		txdata62
9	txdata1		txdata16		txdataRD1		txdata37		txdata53	
8		txdata11		txdata27		txdata32		txdata48		vss
7	txdata0		vss		txdata31		vss		txdata52	
6		txdata12		vss		txdata33		vss		txdata63
5	vss		txdata15		txdata30		txdata36		txdata51	
4		txdata13		txdata28		txdata34		txdata49		txdataRD3
3	txdataRD0		txdata14		txdata29		txdata35		txdata50	
2		vccio		vccio		vccio		vccio		vccio
1	vccio		vccio		vccio		vccio		vccio	
	die edge									

10Col
Recommended for
38-50um bump pitch

	1	2	3	4	5	6	7	8
57	vss		vccio		vccio		vss	
56		vss		vccio		vccio		vss
55	vss		vccio		vccio		vss	
54		rxcksbRD		rxcksb		rxdatasb		rxdatasbRD
53	txdatasbRD		txdatasb		txcksb		txcksbRD	
52		rxdata50		rxdata36		rxdata14		rxdataRD0
51	rxdataRD3		rxdata49		rxdata27		rxdata13	
50		rxdata51		rxdata35		rxdata15		rxdata0
49	vss		rxdata48		vss		rxdata12	
48		rxdata52		rxdata34		rxdata16		vss
47	rxdata63		vss		rxdata28		rxdata11	
46		rxdata53		rxdata33		rxdata17		rxdata1
45	rxdata62		rxdata47		rxdata29		rxdata10	
44		vccio		vccio		vccio		vccio
43	rxdata61		rxdata46		rxdata30		vss	
42		vss		vss		rxdata26		rxdata2
41	rxdata60		rxdata37		rxdata31		rxdata9	
40		rxdata54		rxdata32		rxdata25		rxdata3
39	rxdata59		rxdata38		rxdataRD1		rxdata8	
38		rxdata55		rxdataRD2		rxdata24		rxdata4
37	vss		rxdata39		vss		vss	
36		rxdata45		vss		rxdata23		rxdata7
35	rxdata56		rxdata40		rxckRD		rxdata18	
34		vss		rxvldRD		rxdata22		vss
33	rxdata57		rxdata41		rxckn		rxdata19	
32		rxdata44		rxvld		vss		rxdata6
31	rxdata58		vss		rxckp		rxdata20	
30		rxdata43		rxtrk		rxdata21		rxdata5
29	vss		rxdata42		vss		vss	
28		vccfwdio		vccfwdio		vccfwdio		vccfwdio
27	vccio		vccio		vccio		vccio	
26		vss		vss		txdata42		vss
25	txdata5		txdata21		txtrk		txdata43	
24		txdata20		txckp		vss		txdata58
23	txdata6		vss		txvld		txdata44	
22		txdata19		txckn		txdata41		txdata57
21	vss		txdata22		txvldRD		vss	
20		txdata18		txckRD		txdata40		txdata56
19	txdata7		txdata23		vss		txdata45	
18		vss		vss		txdata39		vss
17	txdata4		txdata24		txdataRD2		txdata55	
16		txdata8		txdataRD1		txdata38		txdata59
15	txdata3		txdata25		txdata32		txdata54	
14		txdata9		txdata31		txdata37		txdata60
13	txdata2		txdata26		vss		vss	
12		vss		txdata30		txdata46		txdata61
11	vccio		vccio		vccio		vccio	
10		txdata10		txdata29		txdata47		txdata62
9	txdata1		txdata17		txdata33		txdata53	
8		txdata11		txdata28		vss		txdata63
7	vss		txdata16		txdata34		txdata52	
6		txdata12		vss		txdata48		vss
5	txdata0		txdata15		txdata35		txdata51	
4		txdata13		txdata27		txdata49		txdataRD3
3	txdataRD0		txdata14		txdata36		txdata50	
2		vccio		vccio		vccio		vccio
1	vccio		vccio		vccio		vccio	
	die edge							

8Col
Recommended for
51-55um bump pitch

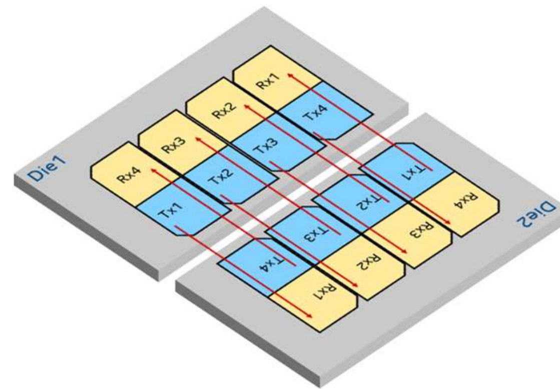
UCIe-A area/column type efficiency plots

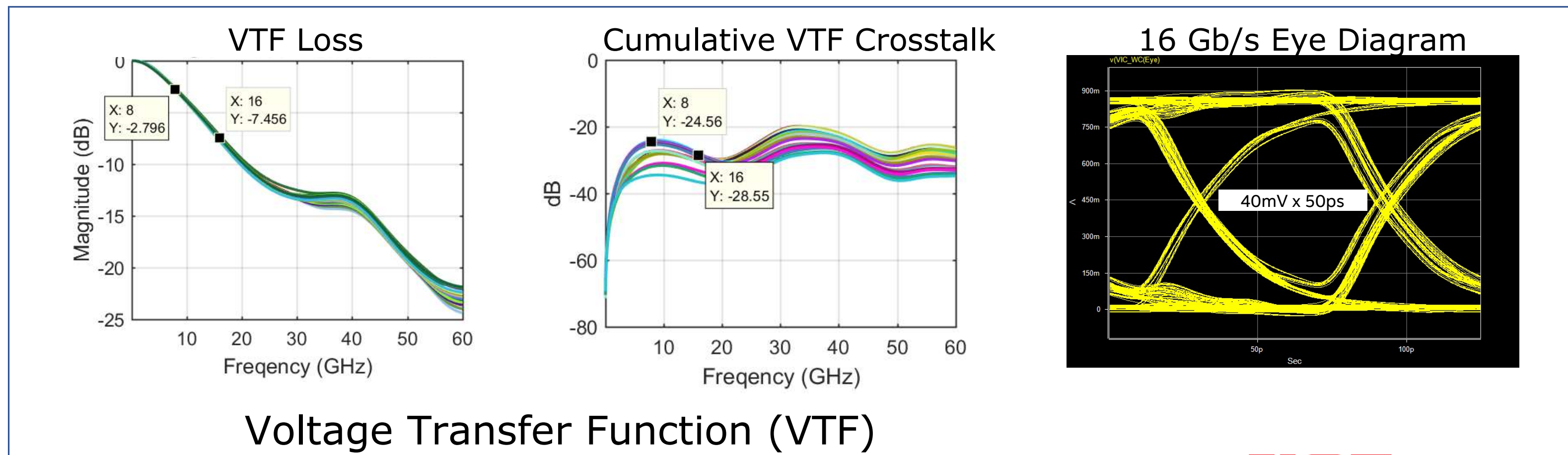


- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps
- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower
- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um)
  - Example: 10% of 1000um is greater than 20% of 400um

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2023

UCIe-A: Arrangement & Channel Characteristics

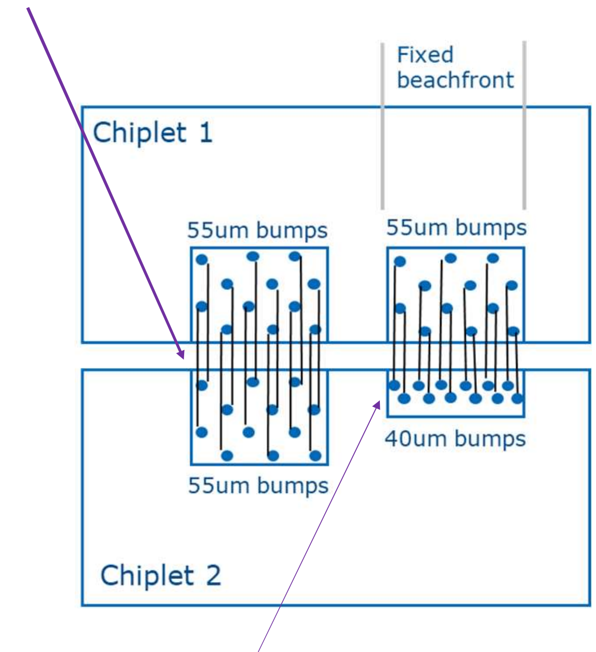




Voltage Transfer Function (VTF)

UCIe-A Interoperability

- Advanced package planning of key parameters up front for interop across IDMs/OSATs:
  - PHY beachfront must be spec to balance BW/mm capability and mechanical compatibility
  - Inter-generational compatibility across bump pitch range
    - Fixed beachfront (388.8um) per PHY module &
    - Signal ordering rules
  - Comprehensive PHY placement & rotation/mirroring rules



- With the reduction of bump pitch, the number of rows decrease while the number of columns increase
- Interop is enabled by a fixed beachfront & following signal ordering rules

UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years across the compute continuum

Compliance Overview

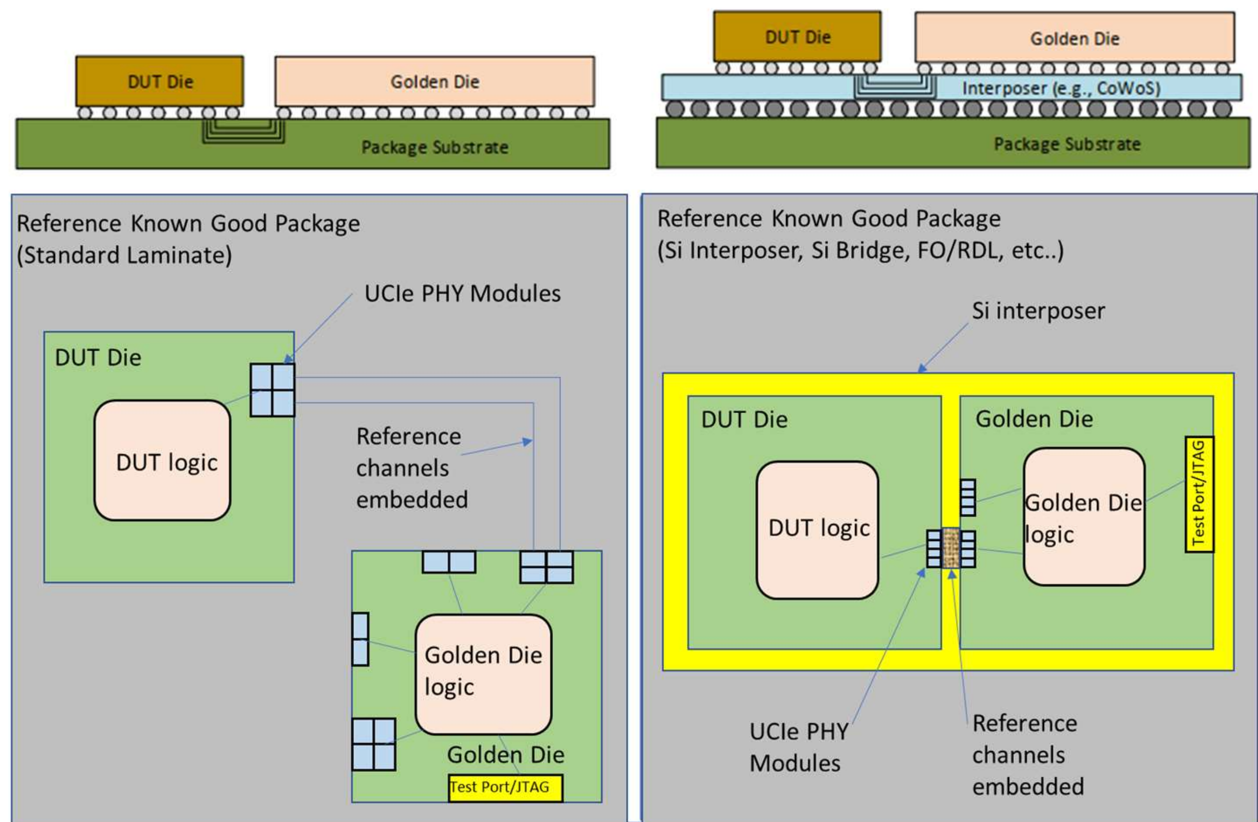
- The goal of Compliance testing is to validate the mainband supported features of a Device Under Test (DUT) against a known good reference UCIe implementation.
- The UCIe sideband link plays a critical role for enabling compliance testing by allowing compliance software to access registers from different UCIe components (e.g. Physical Layer, D2D Adapter, etc.) for setting up tests as well as monitoring status.
- Compliance Test Document to describe:
  - Compliance test setup, including the channel model and package level details
  - Test details
  - Golden Die details including form factor and system-level behavior

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2023

Compliance Setup

Consist of:

- Reference UCIe implementation across all layers of the UCIe stack (Golden UCIe)
- DUT: to be tested with reference design
  - Required to have cleared die sort/pre-bond testing
- For Advanced Package, a known good silicon bridge or interposer.



Protocol and Adapter Compliance

- Protocol Layer Compliance
  - For PCIe and CXL Protocol Layers, UCIe leverage the protocol compliance defined in those specs.
  - For Streaming protocols, Protocol interop is specific to the protocol being streamed, beyond scope of UCIe spec.
- Adapter Compliance:
  - Golden Die Adapter must have all the capabilities defined in UCIe spec, and must have the capability to inject both consistent and inconsistent sideband messages to test DUT for various error scenarios.
  - DUT must have Control and Status registers for
    - Ability to Inject Test or NOP Flits
    - Injection of Link State Request or Response sideband messages
    - Retry injection control

PHY Compliance

- Golden Die must support capabilities to force timeouts on all applicable sideband messages as well as state residence timers.
- Electrical Compliance Features:
  - Timing margining
  - Voltage margining, when supported
  - BER measurement
  - Lane-to-Lane skew for a given module at both RX and TX
  - TX Equalization