Electrical, Form-Factor, and Compliance
Data Rate, BER, and Channel Reach

- **Signaling:** Unidirectional NRZ
- **Data Rate:** 4, 8, 12, 16, 24, 32 Gb/s.
- **Channel Reach:**
  - Advanced Package (25-55um bump pitch):
    - Up to 2mm and 32Gb/s, TX drive control.
    - No RX Termination
  - Standard Package (100-130um bump pitch):
    - TX Termination
    - RX Termination Map
- **BER:**

<table>
<thead>
<tr>
<th>Data Rate (Gb/s)</th>
<th>4</th>
<th>8</th>
<th>12</th>
<th>16</th>
<th>24</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced Package</td>
<td>1.00E-27</td>
<td>1.00E-27</td>
<td>1.00E-27</td>
<td>1.00E-15</td>
<td>1.00E-15</td>
<td>1.00E-15</td>
</tr>
<tr>
<td>Standard Package</td>
<td>1.00E-27</td>
<td>1.00E-27</td>
<td>1.00E-15</td>
<td>1.00E-15</td>
<td>1.00E-15</td>
<td>1.00E-15</td>
</tr>
</tbody>
</table>

Reach for unterminated RX can be increased with higher swing TX

**CRC and Retry for BER 1E-15 to achieve FIT rate <<1**
PHY Architecture

- Basic module data width:
  - x64 for advanced packaging
  - x16 for standard packaging
- Differential Forwarded Clock, Single-Ended Data.
- “Matched” Architecture
  - Better tolerance to power supply noise
- Matched Interconnect Channels
  - Significant power reduction in clock recovery
- SSC allowed, 0 ppm TX to RX
Driver and Input Buffer

TX Driver
- Typical segmented driver
- CMOS implementation shown. NN driver and other structure possible.
- Target source impedance based on optimal eye open, not necessary matching T-Line impedance.
- BW and rise/fall time defined by Rterm and Cpad spec
- TXLE (1-tap de-emphasis) required at 24G+
  - Trained at link-initialization, no realtime adaptation

RX Input Buffer
- Termination (when applicable) is to ground, and matching T-Line impedance.
- Spec does not mandate a specific input buffer design. If RX amplifier is used, recommend BW of > 0.75x data rate (1.5x Nyquist).
- Optional RX CTLE
TX and RX Voltage Compatibility

- Minimum TX swing 0.4V
- Strongly recommend max TX voltage < 0.85V for compatibility with future process nodes

<table>
<thead>
<tr>
<th>Die 1 TX output maximum $V_{OH}$ (V)</th>
<th>$V_{OH}$ - VCC &lt; 0mV</th>
<th>$V_{OH}$ - VCC = 0mV</th>
<th>$V_{OH}$ - VCC &lt; 100mV</th>
<th>$V_{OH}$ - VCC &gt; 100mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die 2 RX AFE VCC level (V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compatibility</td>
<td>Safe</td>
<td>Safe</td>
<td>Safe</td>
<td>Not Safe*</td>
</tr>
</tbody>
</table>

- Cross Process Reliability and Electrical Overstress (EOS) concerns
  - To avoid reliability issues (voltage overstress above allowable process limits: EOS), recommend limiting the TX output high ($V_{OH}$) to a maximum of 100mV above the RX supply rail.
  - When the TX $V_{OH}$ is equal to or lower than the RX AFE supply rail, within ranges in the spec, there won't be reliability concerns.

In the case of “Not Safe*”, RX AFE overstress protection circuitry can be used to mitigate the issue, at cost of area and power consumption.
PHY Clocking Architecture

- Supports 2-way and 4-way interleaving TRX
- Independent even/odd phase control
- Global TX, local TX, local RX phase adjustments depending on data rate.
- Data Valid bit to gate clock distribution (also for data framing)
- Track bit for background training and phase alignment
Dynamic Clock Gating

- Clock gated if Valid remains low after providing postamble
- No clock gating if free running clock mode is negotiated
- Clock parked Hi/Low during alternate clock gating events; 8 UI boundary

UCIE Dynamic Clock Gating (unterminated link example)
Pad Capacitance and ESD

• Cpad has 1st order performance impact
• Aggressive targets on Cpad and ESD
• UCIe 1.0 ESD spec: 30V CDM, further scaling in future, align with Industry Council on ESD Targets.

• T-coil to reduce effective pad capacitance
  • T-coil widely used by serial I/O across industry
  • T-coil size expected to be on the order of 20um x 20um x2

<table>
<thead>
<tr>
<th>TX/RX Pad Capacitance</th>
<th>Advanced Package Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>250/200fF</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TX/RX Pad Capacitance (8Gb/s capable design)</th>
<th>Standard Package Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 fF</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TX/RX Pad Capacitance (16Gb/s capable design)</th>
<th>Standard Package Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 fF</td>
<td>Effective Cpad</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TX/RX Pad Capacitance (32Gb/s capable design)</th>
<th>Standard Package Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>125 fF</td>
<td>Effective Cpad</td>
</tr>
</tbody>
</table>
Other PHY Features

- 800MT/s 2-wire sideband per module
- Global signals (DFX etc.)
- Low Datapath Latency: 12 UI up to 16Gb/s, 16 UI 24-32Gb/s.
- Ultra Fast Idle Exit:
  - L0-idle Power State through Data Valid Clock gating
  - L1 power state (options for further power down)
- Redundancy & Repair for Advanced Package
  - Two per 32 bits
- **Data Scrambling** to mitigate power supply noise

Idle entry/exit details in logic chapter
Channel Specification

• Channel needs to meet minimum eye mask under channel compliance simulation with noiseless jitter-less behavioral TX and RX models

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>4-16Gb/s</th>
<th>24-32Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall (Eye Closure due to Channel)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Eye Height</td>
<td>40mV</td>
<td>40mV</td>
</tr>
<tr>
<td>Eye Width (rectangular eye mask with specified eye height)</td>
<td>0.75 UI</td>
<td>0.65 UI with Equalization Enabled</td>
</tr>
</tbody>
</table>

Insertion loss and Crosstalk spec defined based on the criteria using Voltage Transfer Function (VTF) method

– Due to short transmission line, VTF is more practical than S-parameter based method.
Tightly Coupled Mode

- **Both Conditions must be met:**
  - Shared Power Supply or Forwarded Power Supply
  - Channel supports larger eye mask

- **Rationale / Advantages:**
  - Further Optimization of PHY Circuits to lower power. For example, inverter-based RX, no front amplifier.
  - Reduced Training Complexity, such RX reference voltage training.
  - Preparation for higher density D2D

---

### Data Rate

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>4-16Gb/s</th>
<th>24-32Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall (Eye Closure due to Channel)</td>
<td>40mV</td>
<td>40mV</td>
</tr>
<tr>
<td>Eye Height</td>
<td>0.75 UI</td>
<td>0.65 UI</td>
</tr>
<tr>
<td>Eye Width (rectangular eye mask with specified eye height)</td>
<td>0.75 UI</td>
<td></td>
</tr>
</tbody>
</table>

Eye mask for channel changes to 250mV / 0.7UI for TX swing 0.75V
Up to 16Gb/s
TX and RX Jitters

Specify 1-UI TX jitter, data/clock differential TX jitter, and data/clock differential RX jitter.

\[ E(D_3) = E(D_2) + nT, \quad E \text{ is the mean, } n = 0.5 \text{ for matched arch} \]

Jitter = \( D_1(t-nT) - D_1(t) + D_3(t-nT) - D_2(t) - nT + D_5(t) - D_4(t) \)

\[ \Rightarrow \text{Jitter} = D(t-nT) - D(t) + \delta D_T(t) - nT + \delta D_R(t) \]

where \( D = D_1+D_3 \) (total delay), \( \delta D_T = D_3-D_2 \), \( \delta D_R(t) = D_5-D_4 \)

D1: Tx Common clock delay
D2: Tx Data path clock delay
D3: Tx FWD clock path delay
D4: Rx Data path delay
D5: Rx Clock path delay
Link Timing Analysis

### Timing parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Closure due to Channel</td>
<td>Ch</td>
</tr>
<tr>
<td>Channel Mismatch</td>
<td>Chm</td>
</tr>
<tr>
<td>n-UI TX Total Jitter</td>
<td>Tjnui</td>
</tr>
<tr>
<td>TX Data/Clock Differential Jitter</td>
<td>Tjtx</td>
</tr>
<tr>
<td>TX Duty Cycle Error</td>
<td>Dce</td>
</tr>
<tr>
<td>TX Lane-to-lane Skew Correction Range</td>
<td>Rstx</td>
</tr>
<tr>
<td>TX Lane-to-Lane Skew</td>
<td>Stx</td>
</tr>
<tr>
<td>Clock to Mean Data Training Accuracy</td>
<td>Ekd</td>
</tr>
<tr>
<td>RX Data/Clock Differential Jitter</td>
<td>Tjrx</td>
</tr>
<tr>
<td>Max RX Lane-to-Lane Skew</td>
<td>Msrx</td>
</tr>
<tr>
<td>RX Phase Error</td>
<td>Eph</td>
</tr>
<tr>
<td>Sampling Aperture</td>
<td>Ap</td>
</tr>
</tbody>
</table>

**• Need to meet the following conditions (range defined as peak-to-peak)**

\[
C_h + T_{jnuix} + D_{ce} + S_{tx} + E_{ckd} + T_{jrx} + E_{ph} + A_p \leq 1\text{UI}
\]

\[
C_{hm} \leq R_{stx} - M_{srx}
\]

**• Detailed numbers at different data rates are in the spec and WG discussions**
Link Training and Status State Machine

- Sideband (SB) initialization
  - Initialization and repair (advanced interface) of SB
- Main band (MB) initialization
  - Parameter exchange, CLK, Valid & MB repair & MB reversal
- Main band training
  - Data training, at speed repair/degrade and speed degrade
- Link init
  - Exchange RDI Link management messages
- PHYRETRAIN: Retrain based on Link errors
  - Allow infield repair and degrade
- L1/L2: Lower power state
- Train error: For uncorrectable internal errors and Link down conditions //state timeouts and SB timeouts
- Active: Transactions are sent and received
Main band Initialization

- Data rate set to 4GT/s for main band
- Param
  - Exchange of parameters required to setup maximum speed and other PHY settings
- Cal
  - Perform any required calibration (ex: Tx Duty Cycle, Rx Vref etc.)
- RepairCLK
  - Detect and apply repair (if needed) to clock and track Lanes for Advanced Pkg
  - Functional check of clock and track Lanes for Standard Pkg
- RepairVAL
  - Detect and apply repair (if needed) to Valid Lane for Advanced Pkg
  - Functional check of Valid for Standard Package interface.
- ReversalMB
  - Detect and apply Lane reversal (both Standard and Advanced package)
- RepairMB
  - Detect and apply repair (if needed) for Advanced Pkg interface
  - Functional check and width degrade (if needed) for Standard Pkg interface.
Main band Training

- **VALVREF**
  - Receiver reference voltage (Vref) to sample the incoming Valid
  - Performed through Rx initiated point tests or sweep using Valtrain pattern

- **DataVref**
  - Receiver reference voltage (Vref) to sample the incoming Data
  - Performed through Rx initiated point tests or sweep using LFSR pattern

- **Speed Idle**
  - Frequency changed to highest negotiated Data rate

- **TxSelfCal**
  - UCIe Module calibrates its circuit parameters independent of the UCIe Module Partner

- **RxClkCal**
  - Perform calibration on Clock receive path and align Clock/Track alignment

- **ValTrainCenter**
  - Valid to clock centering and ensure Valid functionality
Main band Training [2]

- **ValTrainVref**
  - Optional operation within the state to allow at speed Vref training on Valid signal
- **DataCenter1**
  - Full Data to clock training with correct Valid framing
  - Tx initiated point tests or eye width sweep with LFSR pattern
- **DataTrainVref**
  - Optional operation within the state to allow at speed Vref training on Data
- **RxDeSkew**
  - Optional Operation within the state to allow Lane-to-Lane skew correction on Rx if needed
- **DataCenter2**
  - Recentering if Rx performs Deskew
- **LinkSpeed**
  - Link stability check; direct Link to repair or speed degrade if needed
- **Repair**
  - Apply repair for Advanced pkg and Width degrade for Standard pkg
# Electrical Summary

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Width</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>64</td>
<td>64</td>
<td>64</td>
</tr>
<tr>
<td>Data Rate (Gb/s)</td>
<td>4-16</td>
<td>4/8/12</td>
<td>16</td>
<td>24/32</td>
<td>4/8/12</td>
<td>16</td>
<td>24/32</td>
</tr>
<tr>
<td>Power Efficiency Target (pJ/b)</td>
<td>0.25-0.5</td>
<td>0.5-1</td>
<td>0.5-1</td>
<td>0.75-1.25</td>
<td>0.25-0.5</td>
<td>0.3-0.6</td>
<td>0.3-0.6</td>
</tr>
<tr>
<td>Latency Target (TX+RX) (UI)</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>16</td>
<td>12</td>
<td>12</td>
<td>16</td>
</tr>
<tr>
<td>Idle Power (% of peak)</td>
<td>15%</td>
<td>15%</td>
<td>15%</td>
<td>15%</td>
<td>15%</td>
<td>15%</td>
<td>15%</td>
</tr>
<tr>
<td>Channel Reach (mm)</td>
<td>2-10</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Die Edge BW Density (GByte/s/mm)</td>
<td>28-112</td>
<td>28-84</td>
<td>112</td>
<td>168/224</td>
<td>165/494</td>
<td>658</td>
<td>988/1317</td>
</tr>
<tr>
<td>BW Area Density (GByte/s/mm²)</td>
<td>21-85</td>
<td>21/42/64</td>
<td>85</td>
<td>109/145</td>
<td>158/316/473</td>
<td>631</td>
<td>710/947</td>
</tr>
<tr>
<td>PHY dimension Width (um)</td>
<td>571.5</td>
<td>571.5</td>
<td>571.5</td>
<td>571.5</td>
<td>388.8</td>
<td>388.8</td>
<td>388.8</td>
</tr>
<tr>
<td>PHY dimension Depth (um)</td>
<td>1320</td>
<td>1320</td>
<td>1320</td>
<td>1540</td>
<td>1043</td>
<td>1043</td>
<td></td>
</tr>
<tr>
<td>ESD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>30V CDM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Advanced package PHY depth depends on bump pitch, number based on 45um

(Further scaling in future, align with Industry Council on ESD Targets)
Coffee Break
UCIe 1.0: Supports Standard and Advanced Packages

- Standard Package: 2D – cost effective, longer distance
- Advanced Package: 2.5D – power-efficient, high bandwidth density
- Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer

<table>
<thead>
<tr>
<th>CHARACTERISTICS</th>
<th>STANDARD PACKAGE</th>
<th>ADVANCED PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate (GT/s)</td>
<td>4, 8, 12, 16, 24, 32</td>
<td></td>
</tr>
<tr>
<td>Width (each cluster)</td>
<td>16</td>
<td>64</td>
</tr>
<tr>
<td>Bump Pitch (um)</td>
<td>100 – 130</td>
<td>25 - 55</td>
</tr>
<tr>
<td>Channel Reach (mm)</td>
<td>&lt;= 25</td>
<td>&lt;=2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>KPIs / TARGET FOR KEY METRICS</th>
<th>STANDARD PACKAGE</th>
<th>ADVANCED PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>B/W Shoreline (GB/s/mm)</td>
<td>28 – 224</td>
<td>165 – 1317</td>
</tr>
<tr>
<td>B/W Density (GB/s/mm²)</td>
<td>22-125</td>
<td>188-1350</td>
</tr>
</tbody>
</table>

UCIe 1.0 spec supports multiple packaging technology options to build an open ecosystem
UCIe-S: Standard Package Bump Maps

- Two options: x16 and x32 bump arrangements for BW/mm flexibility
  - 4-2-4 recommended package stack-up for x16 (two topside stripline routing layers)
  - 8-2-8 recommended package stack-up for x32 (4 topside stripline routing layers) for doubled BW/mm
UCIe-S: Arrangement & Channel Characteristics

- 2-module stacking
- 18 IO/mm/layer
- 2 routing layers for each module
- 4 routing layers for 2 modules
- power
ground
signals on L8
signals on L6
signals on L4 and L2 not shown

Voltage Transfer Function (VTF)

25mm length

32Gb/s Eye Diagram
UCIe-A Bump Maps

- Bumpout configurations for maintaining optimized BW/mm² across allowable bump pitch range
  - 8, 10 and 16-columns
  - Suggested usage guideline:

<table>
<thead>
<tr>
<th>BP</th>
<th>Max Data Rate by Spec</th>
<th>Columns within 388.8 shoreline</th>
</tr>
</thead>
<tbody>
<tr>
<td>25-30</td>
<td>12</td>
<td>16</td>
</tr>
<tr>
<td>31-37</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>38-44</td>
<td>24</td>
<td>10</td>
</tr>
<tr>
<td>45-50</td>
<td>32</td>
<td>8</td>
</tr>
<tr>
<td>51-55</td>
<td>32</td>
<td>8</td>
</tr>
</tbody>
</table>

- **16Col**
  - Recommended for 25-37um bump pitch

- **10Col**
  - Recommended for 38-50um bump pitch

- **8Col**
  - Recommended for 51-55um bump pitch

Max Data Rate 12

Recommended for 25-37um bump pitch

Recommended for 38-50um bump pitch

Recommended for 51-55um bump pitch
UCIe-A area/column type efficiency plots

- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps.

- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower.

- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um).
  - Example: 10% of 1000um is greater than 20% of 400um.
UCIe-A: Arrangement & Channel Characteristics

Voltage Transfer Function (VTF)

16 Gb/s Eye Diagram

40mV x 50ps
UCIe-A Interoperability

- Advanced package planning of key parameters up front for interop across IDMs/OSATs:
  - PHY beachfront must be spec to balance BW/mm capability and mechanical compatibility
  - Inter-generational compatibility across bump pitch range
    - Fixed beachfront (388.8um) per PHY module &
    - Signal ordering rules
  - Comprehensive PHY placement & rotation/mirroring rules

UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years across the compute continuum

- With the reduction of bump pitch, the number of rows decrease while the number of columns increase
- Interop is enabled by a fixed beachfront & following signal ordering rules
Compliance Overview

• The goal of Compliance testing is to validate the mainband supported features of a Device Under Test (DUT) against a known good reference UCIe implementation.

• The UCIe sideband link plays a critical role for enabling compliance testing by allowing compliance software to access registers from different UCIe components (e.g. Physical Layer, D2D Adapter, etc.) for setting up tests as well as monitoring status.

• Compliance Test Document to describe:
  • Compliance test setup, including the channel model and package level details
  • Test details
  • Golden Die details including form factor and system-level behavior
Compliance Setup

Consist of:

• Reference UCIe implementation across all layers of the UCIe stack (Golden UCIe)
• DUT: to be tested with reference design
  • Required to have cleared die sort/pre-bond testing
• For Advanced Package, a known good silicon bridge or interposer.
Protocol and Adapter Compliance

• Protocol Layer Compliance
  • For PCIe and CXL Protocol Layers, UCle leverage the protocol compliance defined in those specs.
  • For Streaming protocols, Protocol interop is specific to the protocol being streamed, beyond scope of UCle spec.

• Adapter Compliance:
  • Golden Die Adapter must have all the capabilities defined in UCle spec, and must have the capability to inject both consistent and inconsistent sideband messages to test DUT for various error scenarios.
  • DUT must have Control and Status registers for
    • Ability to Inject Test or NOP Flits
    • Injection of Link State Request or Response sideband messages
    • Retry injection control
PHY Compliance

- Golden Die must support capabilities to force timeouts on all applicable sideband messages as well as state residence timers.

- Electrical Compliance Features:
  - Timing margining
  - Voltage margining, when supported
  - BER measurement
  - Lane-to-Lane skew for a given module at both RX and TX
  - TX Equalization