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A Heterogeneous SoC for Bluetooth LE in 28nm

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Abstract

OsciBear is a system-on-chip (SoC) featuring a RISC-V 32-bit 5-stage in-order scalar processor, AES accelerator, BLE 1M baseband-modem, and a 2.4 GHz radio front end (RFE) transceiver. It was designed in TSMC's 28nm process with a total die area of 1 mm^2 during the course of a 14-week semester by 18 students - 4 Ph.D students, 6 masters students, and 8 undergraduates – enrolled in UC Berkeley's special topics course "28nm SoC for IoT" in Spring 2021. Additionally, a PCB was designed with off-chip reference clocks, bring-up tooling, as well as power amplifiers, RF switch, and an antenna to complete the radio front-end.

The CPU has been demonstrated to run up to 30 MHz in typical operating conditions. The BLE 1M-compliant PHY layer packet assembly and disassembly has been verified in-hardware through "loopback" testing. Adherence to BLE's PHY FM specifications has also been verified with a commercial BLE receiver. In total, the chip consumes 8.43 mW of static power.

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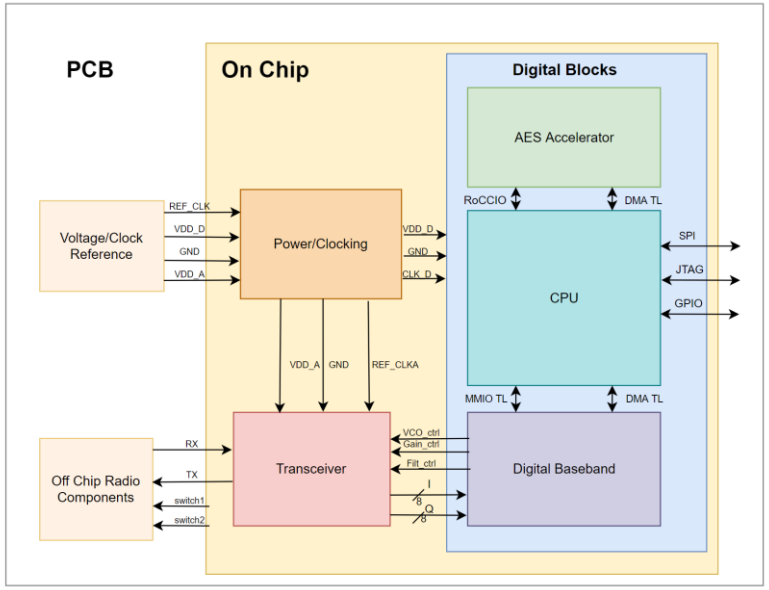
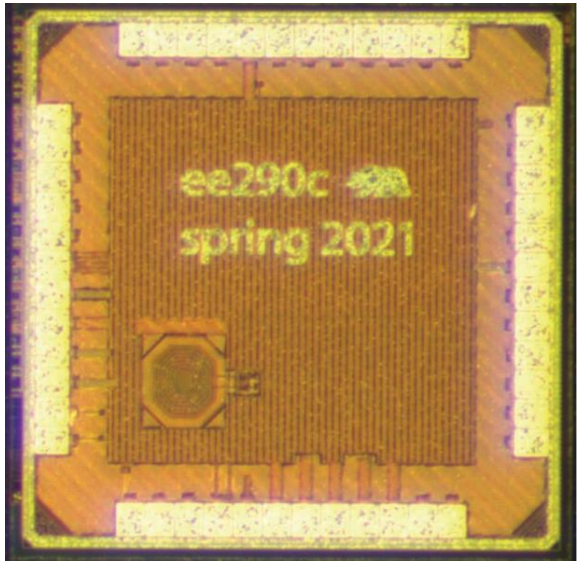
Motivation

- Create a system-on-chip (SoC) (dubbed OsciBear) featuring:
  - RISC-V 32-bit 5-stage in-order scalar processor
  - AES accelerator
  - BLE 1M baseband-modem
  - 2.4 GHz radio front end (RFE) transceiver
  - On chip power regulation and distribution
- Tape out in 14 weeks with 19 students (4 Ph.D students, 6 masters students, and 8 undergraduates)
- Demonstrate Berkeley developed agile hardware tools and flow
- More about UC Berkeley's tapeout course can be found at https://ucb-ee290c.github.io





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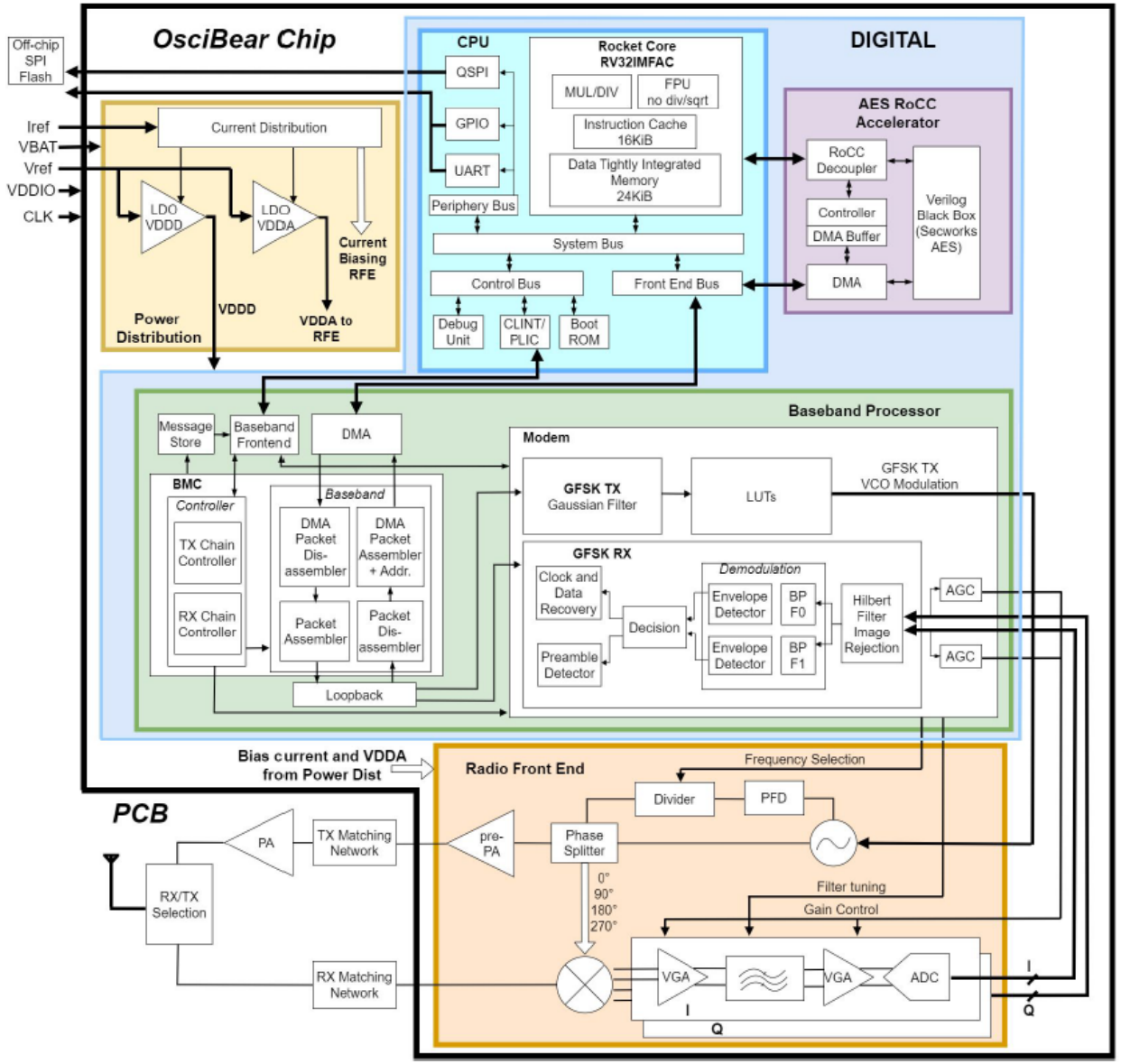
Chip Architecture



- Digital Components
  - Compute
    - RV32IMAFC Core
    - Interrupt Controller
    - UART and TSI peripherals
  - Digital Baseband
    - TX/RX packet control
    - Digital RF tuning constants
- Analog Components
  - Radio Front End
    - Low-IF receiver architecture
    - Transmitter and LO generation through VCO
    - Digital GFSK modulation tuning interface
  - Power Regulation
    - Analog, digital, and I/O domains
    - LDOs for analog and digital domains
- <10mW of static power
- 74% density on digital portion of chip

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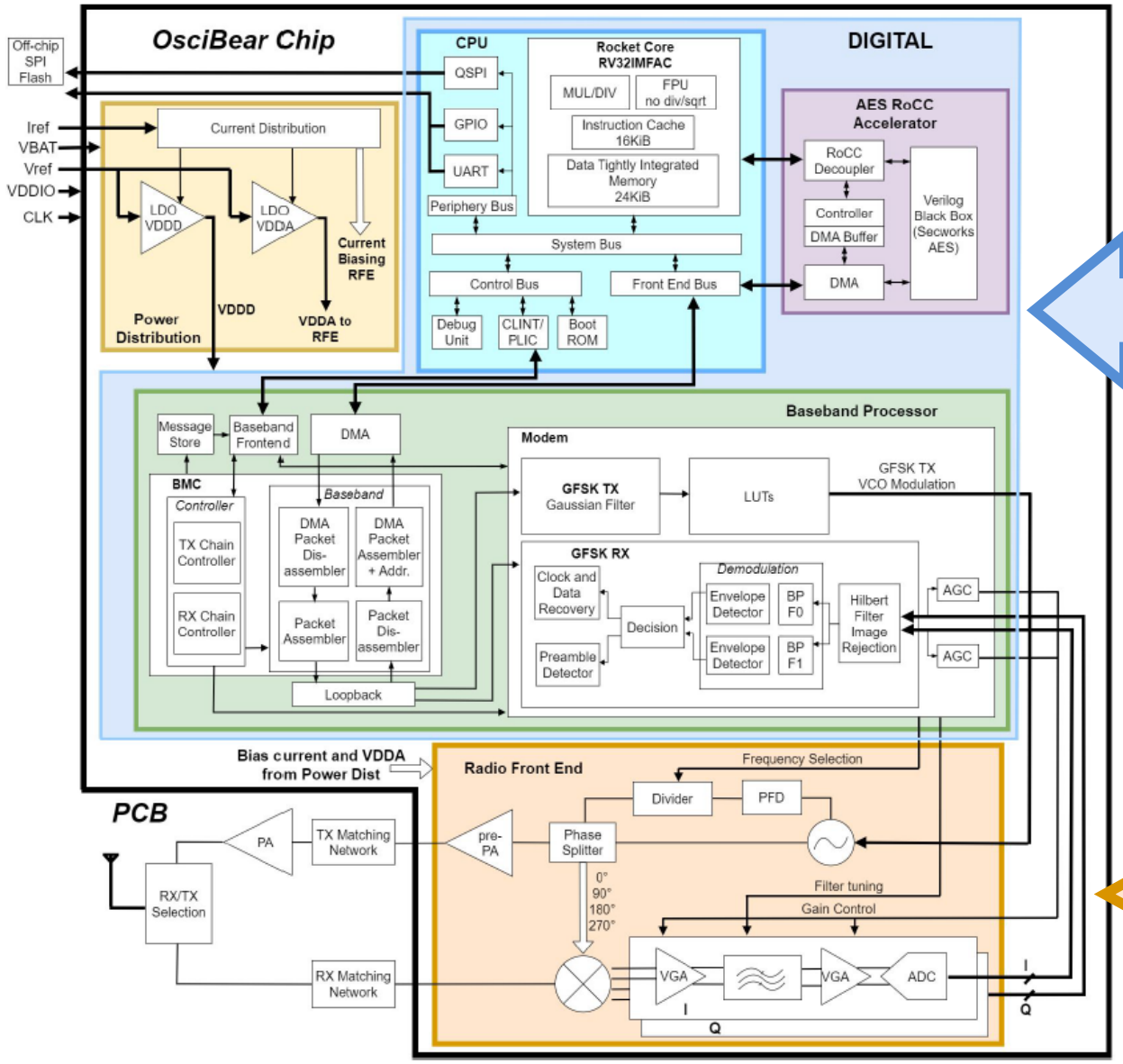
Research Infrastructure



CHIPYARD
https://chipyard.readthedocs.io

HAMMER
https://hammer-vlsi.readthedocs.io

CHISEL
https://www.chisel-lang.org

BAG
Berkeley Analog Generator
(ADC Only)
https://bag3-readthedocs.readthedocs.io

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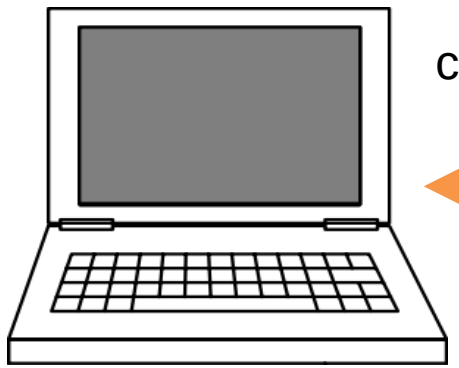
Verification

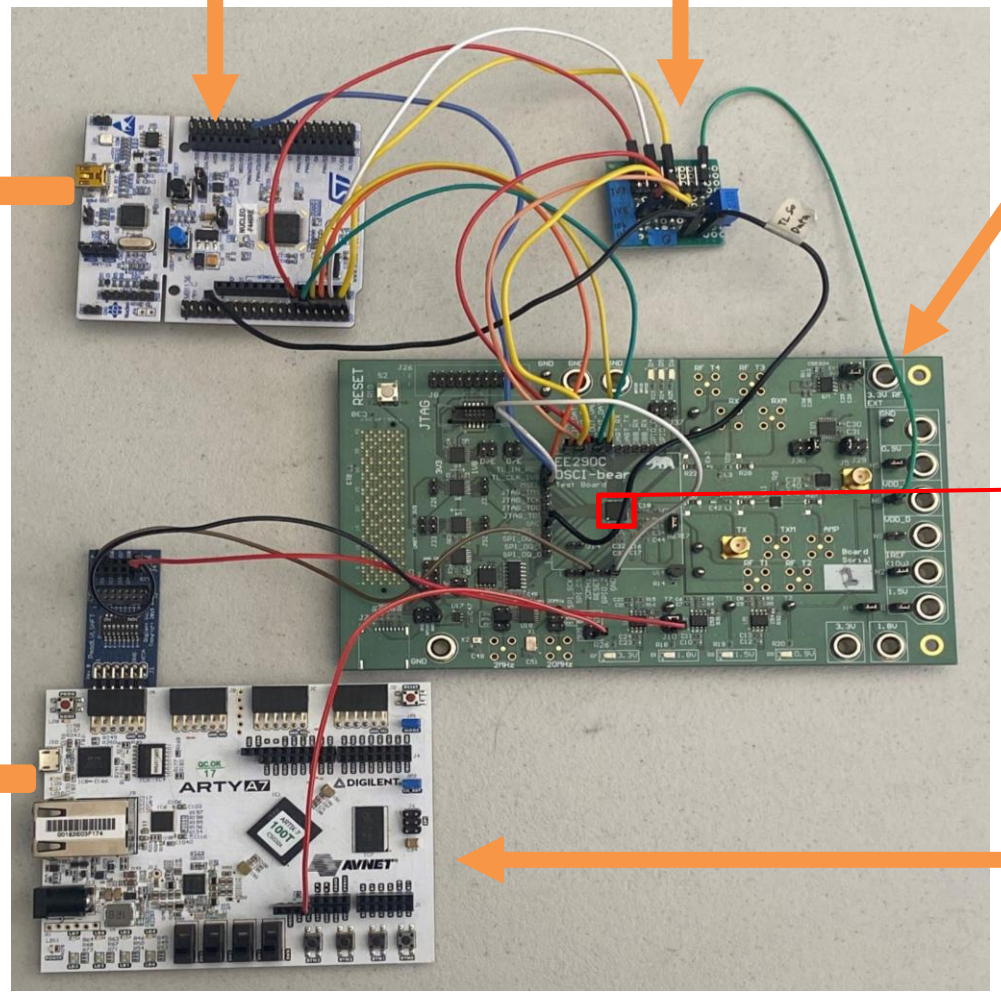
ST32 microcontroller programming chip through Tilelink interface

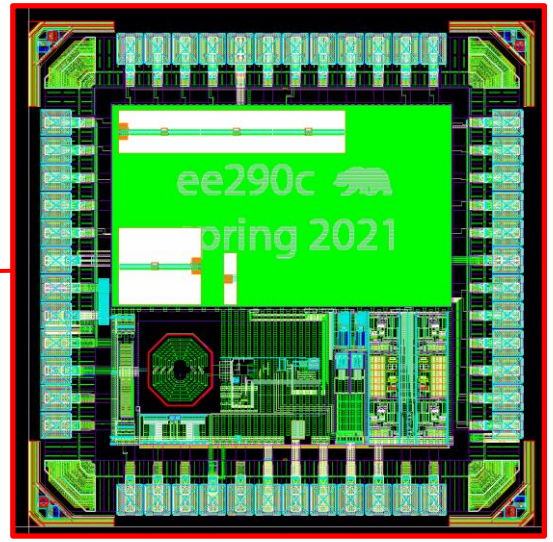
Current tuning board

Student designed PCB

USB connection to laptop







Arty A7 FPGA providing CPU clock and power

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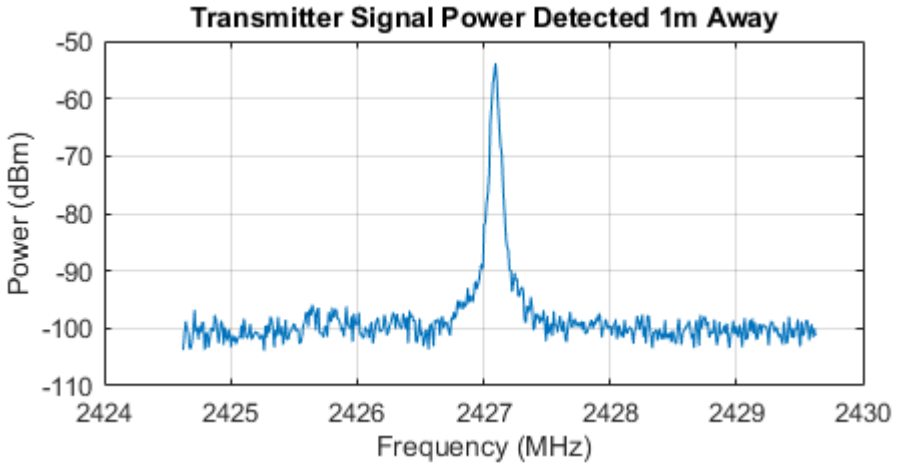
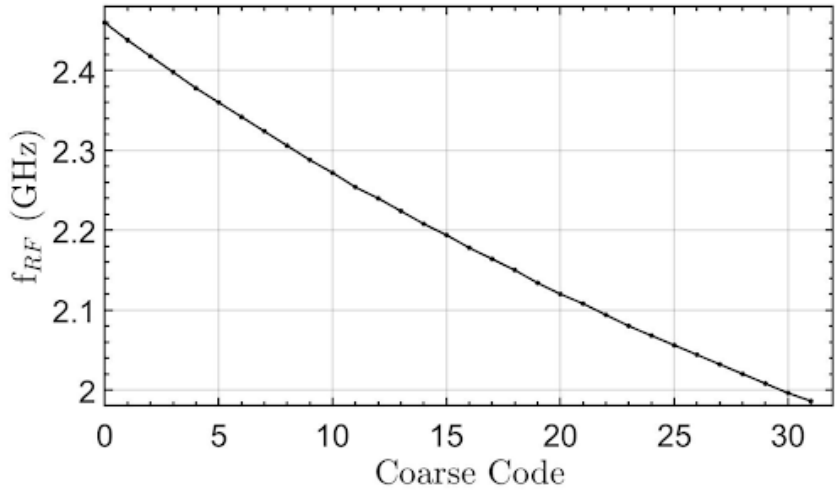
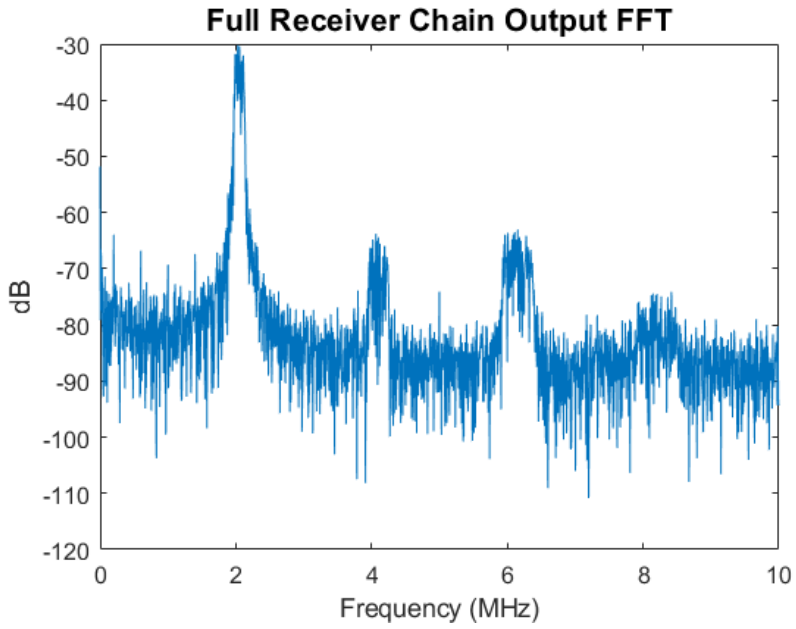
BLE Transceiver Analog Measurements

- Receiver tested from PCB antenna port to differential output of final VGA (pre-ADC)
- Transmitter measured using antennas spaced approximately 1 meter away





LO tuning through digital calibration

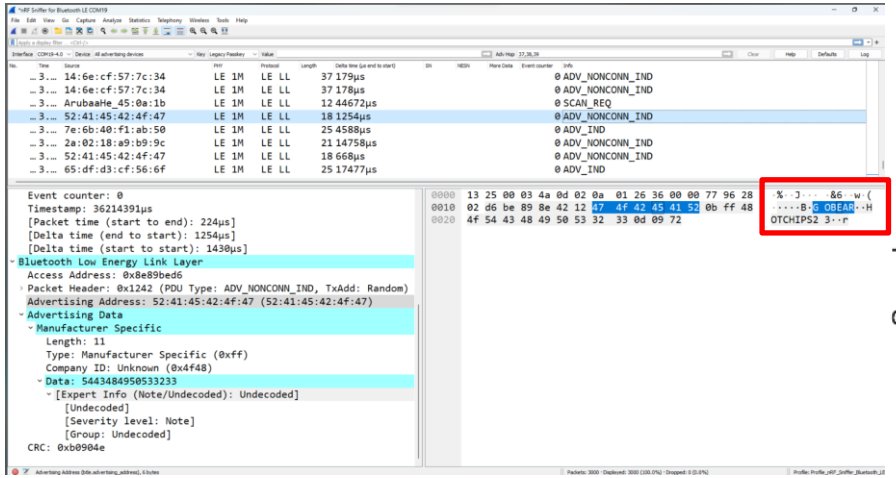


Radio Measurement Summary	
TX Frequency Modulation Range	~250 kHz
TX Power 1 meter away	-55 dBm
RX Chain SNDR (pre-ADC)	24.87 dB

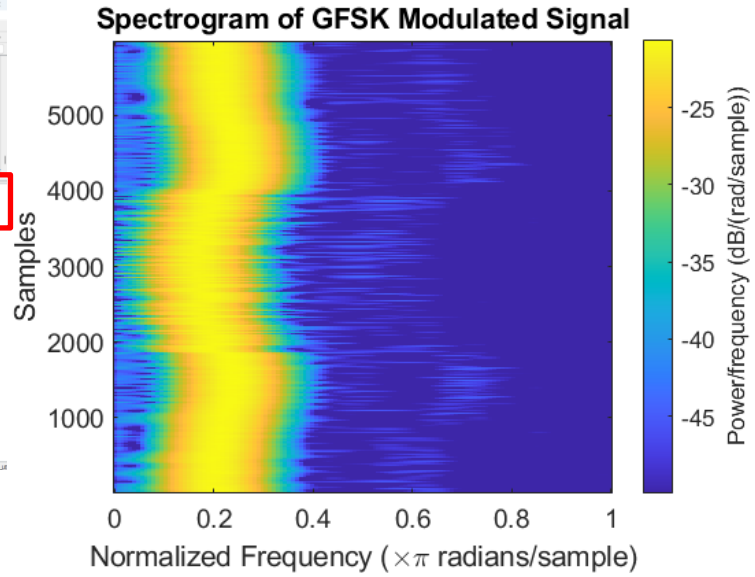
BLE Transmitter Measurement

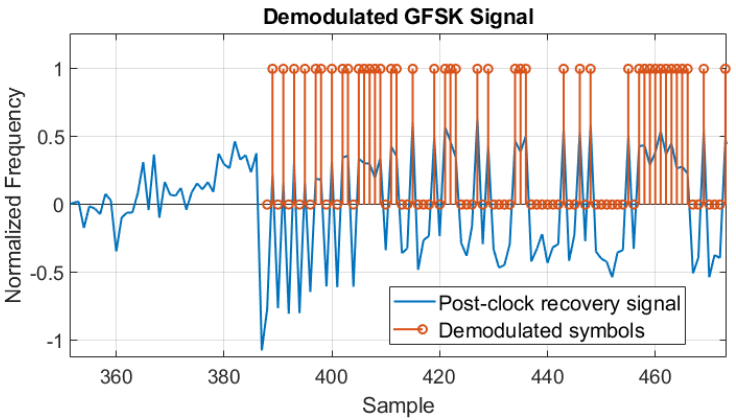
Transmit packet decoding done two ways:

1. Software Testing
   - Transmitted RF signal mixed down off chip
   - IF signal demodulated in software showed preamble, access address, and payload
2. Commercial (Nordic nRF52840 DK) receiver
   - LO calibrated to BLE channel 38 (advertisement)
   - Packet transmitted periodically with commercial receiver configured as sniffer



Commercial receiver decoding correctly formed packet sent with "GOBEAR HOTCHIPS23" as payload





Demodulation in software

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Video Demo

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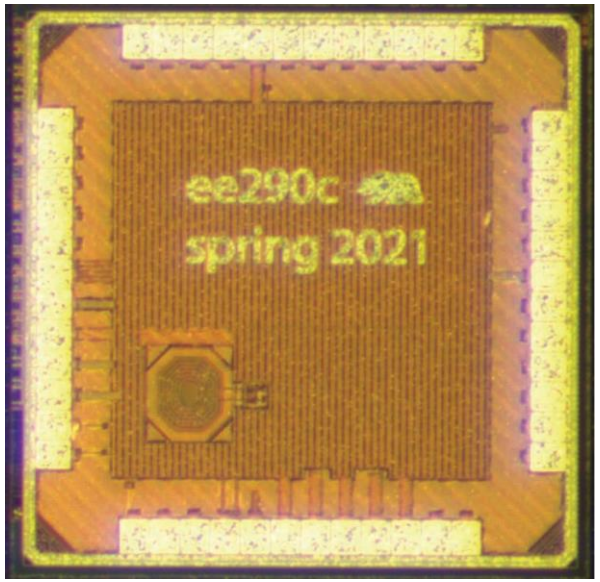
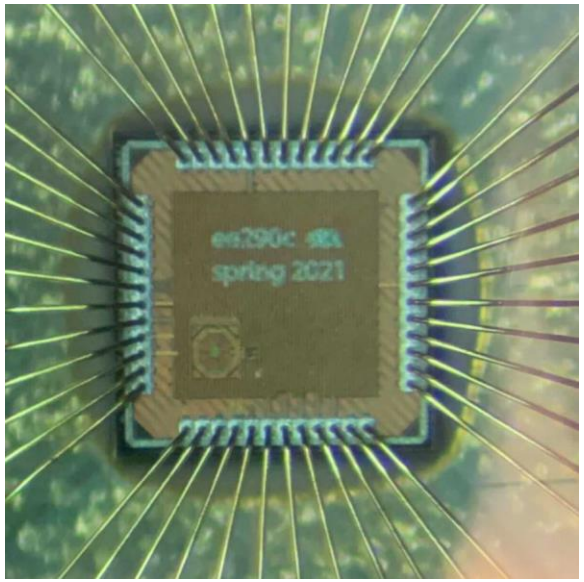
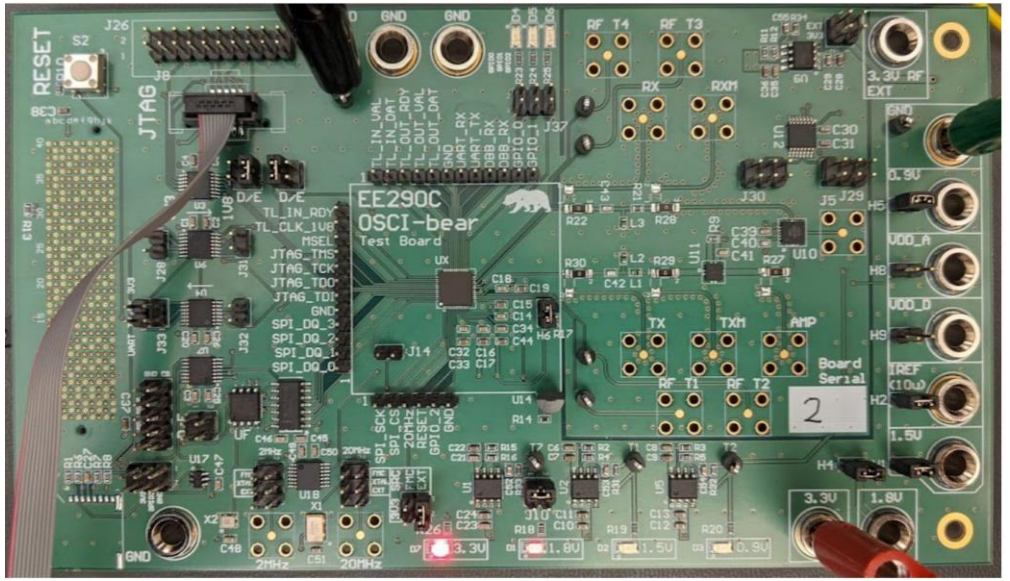
Conclusion

- Completely student driven chip design and bringup
- Successfully designed and tested SoC featuring BLE radio, with verified:
  - RISC-V 32-bit IMAC instructions
  - DMA controller
  - BLE 1M Digital Baseband Modem
  - RF Frontend
  - Power distribution with on chip LDO regulation
- More about the design process and this iteration of the course can be found in our prior publication:
  Tape-Out Course: Silicon in a Semester







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Acknowledgements

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