

An Open-Source 130-nm Fusion-Enabled Deconvolution Kernel Generator IC For **Real-Time mmWave Radar Platform Motion Compensation** 

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### **Existing Sensor Networks and Systems** Analog • Perception via **passive** silicon ICs (e.g., mmWave radars) with Accelerometer resource-intensive post-processing information extraction. Sensing on Edge Devices Input • Requires reduced computational cost and resource consumption.

• Reduced latency and increased throughput  $\rightarrow$  real-time perception.

# **Challenge**

- Parasitic platform motion degrades resolution and sensing capacity.
- Existing solutions operate in post-processing  $\rightarrow$  resource-intensive, not real-time.

MOTIVATION





# **CHIPARCHITECTURE**

High-pass-filtered *x*-axis signal from an analog accelerometer.

## Analog Front-End

- Process the frequency and amplitude of the accelerometer-detected platform vibration and digitize the results via separate SAR ADCs.
- External frequency-detect circuitry to bypass a non-functional PLL.

# **DSP Back-End**

- Formulate + store in memory the estimated deconvolution kernel.
- Transfer function coefficient lookup + an optimized frequency response evaluation pipeline yield time- and energy-efficient kernel estimation.

### Output

<u>Input</u>

Digital deconvolution kernel frequency response (phase + magnitude).

# **DECONVOLUTION KERNEL GENERATION**

We present the first custom IC dedicated to enabling **real-time**, **resource-efficient** FMCW mmWave radar platform vibration compensation, via early sensor fusion.

- Accelerometer fusion: chip detects frequency and amplitude of vibration.





Increasing target velocity toward radar.

**Performance Summary** 



	This Work	[1]	[2]	[3]	[4]
Key Features	Fusion-aided real-time platform compensation for FMCW mmWave radar.	Wideband analog/RF SIC via LMS with autonomous adaptation to time-varying interference channels.	Continuous-time LMS adaptive filter of TX leakage in CDMA receivers.	Broadband SIC via Hilbert transform equalization (HTE) implemented in baseband.	RF + analog BB on-chip SIC via adaptive adjustment of cancellation signal + off-chip nonlinear digital BB cancellation.
Suppression Domain	Analog + Digital	Analog	Analog	Analog	Analog + Digital
Interference Suppression	26-35 dB	24 dB	14-21 dB	23 dB	20 dB
Computational Complexity	Second-order digital IIR deconvolution kernel, lookup-based, point-wise mult. correction $\rightarrow$ <i>minimal</i> <i>computation</i> .	Analog LMS adaptive circuitry only – no additional off-chip digital calibration, single tap per canceller $\rightarrow$ <i>minimal</i> <i>computation</i> .	Analog LMS adaptive circuitry only – no additional off-chip digital calibration $\rightarrow$ <i>minimal</i> <i>computation</i> .	Minimal number of equalizer taps via baseband HTE after RF downconversion + LPF → minimal computation.	Adaptive transmit interference cancellation; gradient descent to adapt amplitude, phase, and delay $\rightarrow$ <i>computationally</i> <i>complex</i> .
Bandwidth	12.5 MHz <sup>†</sup>	20 MHz	1 MHz	80 MHz	20 MHz
Canceller Power Consumption	2.43 mW	66 mW	30.5 mW	13 mW	80 mW
Fechnology	130-nm CMOS	65-nm CMOS	250-nm CMOS	130-nm CMOS	65-nm CMOS
Active Area	$10.28 \text{ mm}^2$	$3 \text{ mm}^2$	$1.3 \text{ mm}^{2}$ §	$0.72 \text{ mm}^2$	$3.24 \text{ mm}^2$
# Channels	1 TX, 1 RX	1 TX, 1 RX	1 TX, 1 RX	1 TX, 1 RX	1 TX, 1 RX

# References

[1] Y. Cao, *JSSC*'20. [2] V. Aparin, *JSSC*'06. [3] A. El Sayed, *TCAS-I*'19. [4] S. Ayati, *TCAS-I*'21.