HotChips 2023

Intel Agilex® 9 Direct RF-Series FPGAs with Integrated 64 Gsps Data Converters

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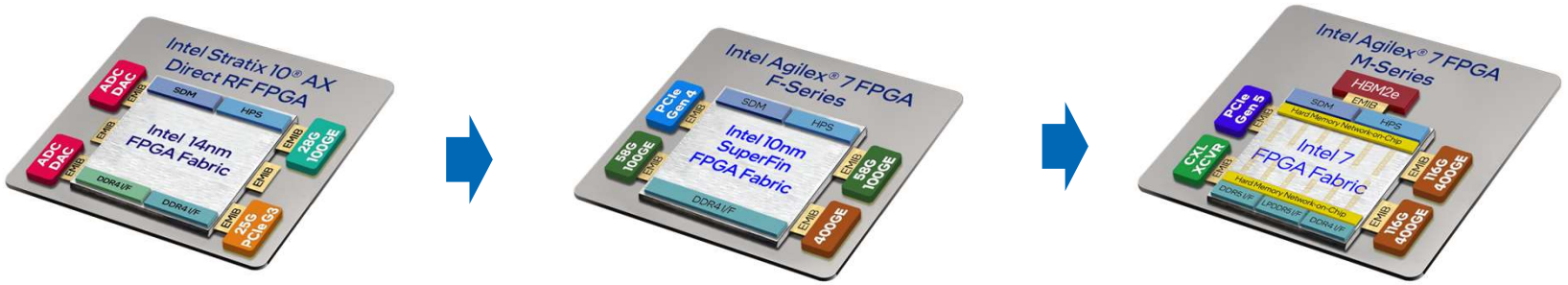
Agenda

- Intel Heterogeneously Integrated FPGAs
- Intel Agilex® FPGA Derivatives
- Intel Agilex® Direct RF-Series FPGA Product Offering
- 64 Gsps Wideband Direct RF-Series FPGA Architecture
- 64 Gsps Wideband Direct RF-Series FPGA Test Results
- Development Tools / Reference Designs
- Future Potential Chiplet-Based FPGAs
  - UCIe: Next-Generation Chip-to-Chip Interface

Intel Heterogeneously Integrated FPGAs

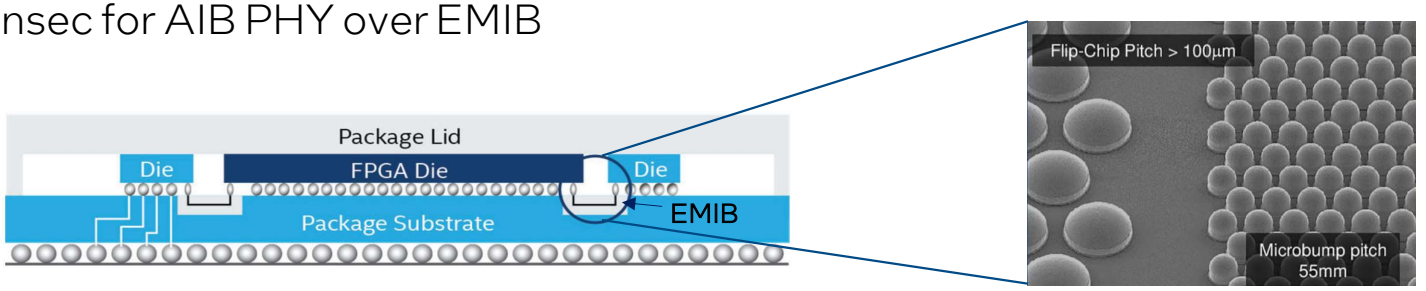
- Intel® Stratix 10® and Intel Agilex® FPGAs are heterogeneously integrated (HI) multi-chip packages (MCPs)
- Supports multi-foundry / multi-process node integration
  - Select node for cost / performance requirements, i.e., analog
- Rapid upgrade when new tile is developed



10 Different Chiplets, 4 Different Foundries, 7 Process Nodes, 2 External Partners

Intel Heterogeneously Integrated FPGAs

- Leverage Intel Embedded Multi-die Interconnect Bridge (EMIB)
  - Higher performance, shorter length, lower cost versus interposer
- Utilize AIB[1] open standard as physical layer (PHY)
- Intel's AIB/EMIB interface
  - High parallelism: Up to 1920 wires per AIB interface
  - High bandwidth: Up to 960 Gbps per interface (Up to six on an FPGA die)
  - Low power: 0.8pJ/bit (Intel Agilex® FPGAs)
  - Low latency: <4nsec for AIB PHY over EMIB



[1]Advanced Interconnect Bus (AIB) can be used with interposer, silicon bridge, Intel uses EMIB for chip-to-chip connection

Expanding Chiplet Ecosystem

- Intel internal development
  - FPGAs, connectivity and other chiplets
- Third-party chiplet development
  - Data converters, security, connectivity
- Government investment via SHIP*
  - Contract to develop and demonstrate access to state-of-the-art (SOTA) heterogeneous integrated packaging (HIP) technology
  - Enable path to custom Multi-chip packages (MCPs) for Defense Industrial Base (DIB) Customers

Technology & Foundry Agnostic

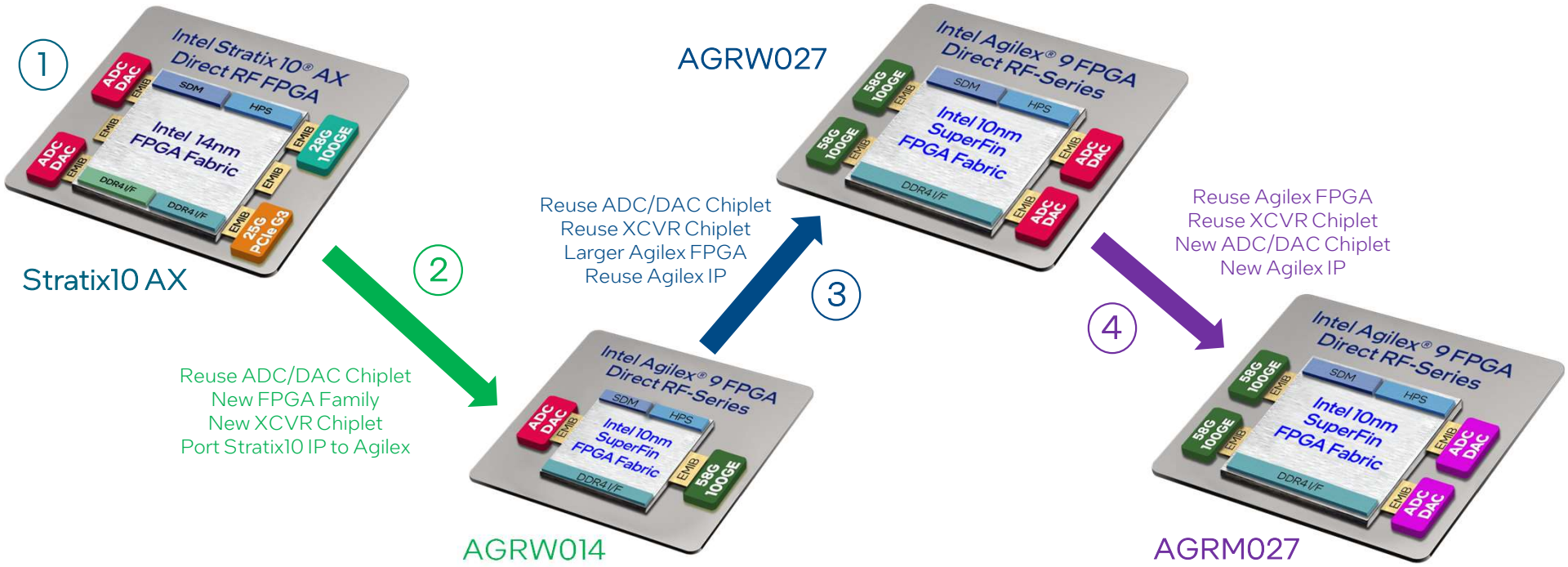
- 2 FPGA Families
- 6 XCVR/SERDES Chiplets
- 3 Data Converter Chiplets
- 3 Optical Chiplets
- 2 Compute Chiplets
- 6 Defense Industrial Base Chiplets

3 Foundries, 9 Process Nodes

* State-of-the-Art Heterogenous Integrated Packaging (SHIP), Navy Surface Warfare Center, Crane Government Contract, SHIP Phase 2,

Composable Chiplet Solution Example: Direct RF FPGAs

- Standardization and reuse accelerates product rollout



Intel Agilex® Heterogenous FPGA Derivatives*

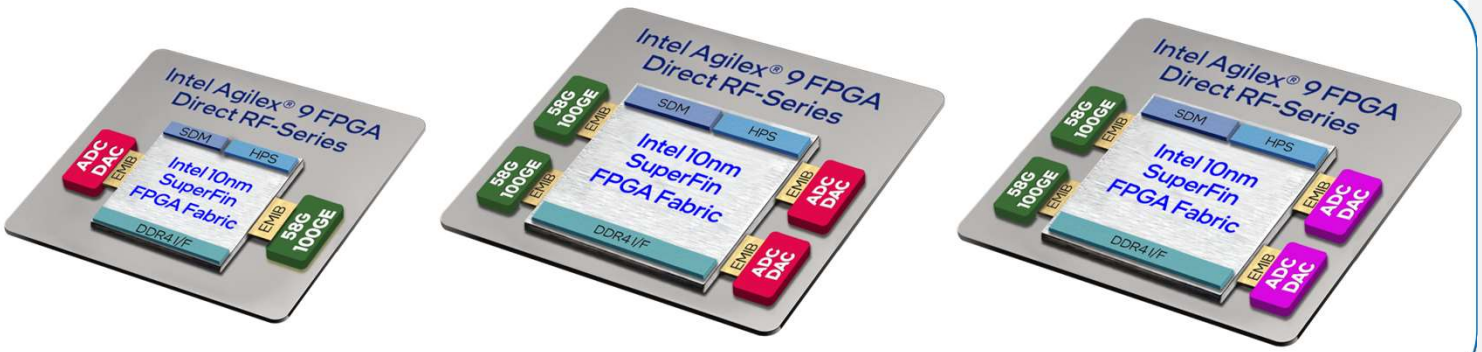
~2X Increased
Fabric Performance per Watt[1,4]

Average 50%
Higher Performance[2,4]

Up to 40%
Lower Power[2,4]

Up to 40 TFLOPs
DSP Performance[3,4]

Intel Agilex® 7 F-Series, I-Series, M-Series FPGAs



Intel Agilex® 9 Direct RF-Series FPGAs

[1] Compared to competing 7 nanometer FPGA
[2] Compared to Intel® Stratix® 10 FPGAs
[3] With FP16 configuration
[4] Based on current estimates
See FPGA - Performance Index for workloads and configurations. Results may vary.

* Other FPGA die / chiplet combinations available

Intel Agilex® Heterogenous FPGA Derivatives*

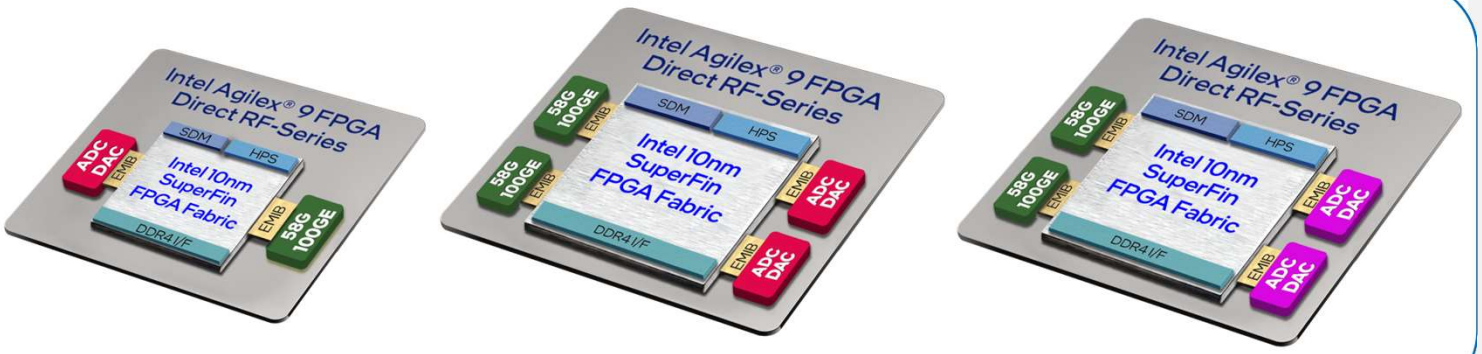
10 Different Chiplets

4 Different Foundries

5 Different Process Nodes

3 External Partners

Intel Agilex® 7 F-Series, I-Series, M-Series FPGAs



Intel Agilex® 9 Direct RF-Series FPGAs

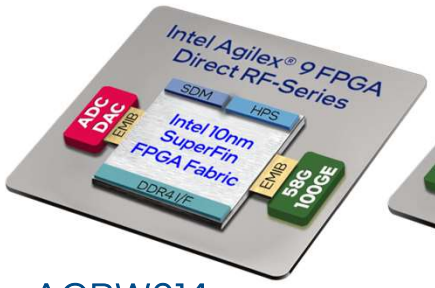
*Other FPGA die / chiplet combinations available

Intel Agilex® 9 Direct RF-Series FPGAs

Wideband FPGAs

Up to Eight 64 Gsps ADCs

Up to Eight 64 Gsps DACs



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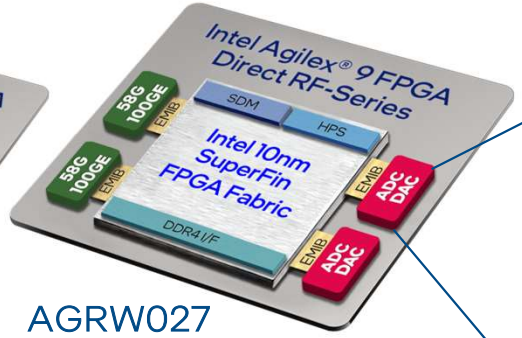

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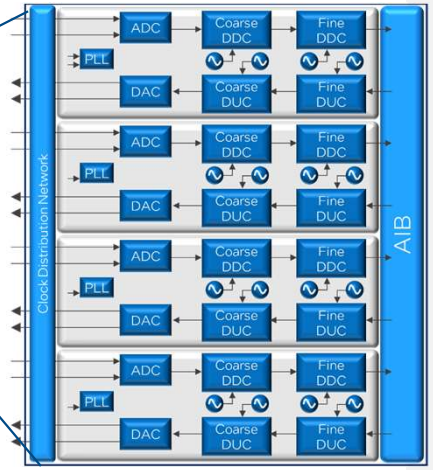
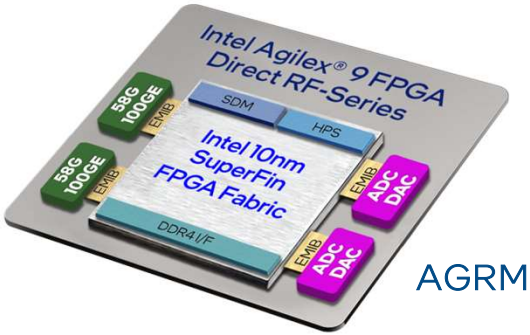
Wideband Data Converter Chiplet



Medium Band FPGA

Twenty 4 Gsps ADCs

Sixteen 12 Gsps DACs

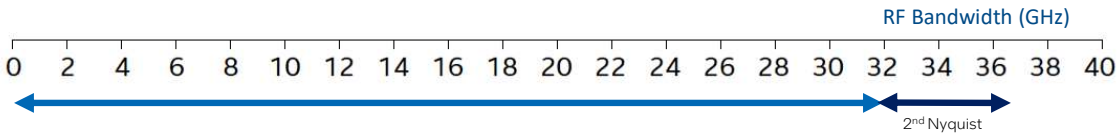


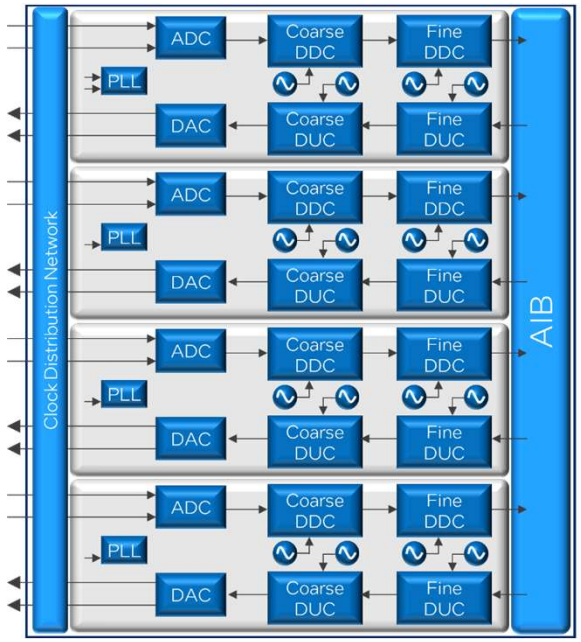
AGRM027

[1] Other FPGA die / chiplet combinations available

Wideband 64 GSPS Data Converter Tile (DCT) Overview

- Quad 40-64 GSPS Data Converter Tiles (DCT)
  - Full duplex, 4TX / 4RX
- Frequency agile across entire spectrum
  - Plus, operation into 2nd Nyquist
- Wideband mode supports full 32 GHz of IBW
  - Reference designs show 64 GSPS processing in FPGA
- Programmable Digital Up/Down Converters
  - 1x (ADC Only), 8x-1024x
- Synchronization to support beam forming
  - Single Device or multi-device reference designs available

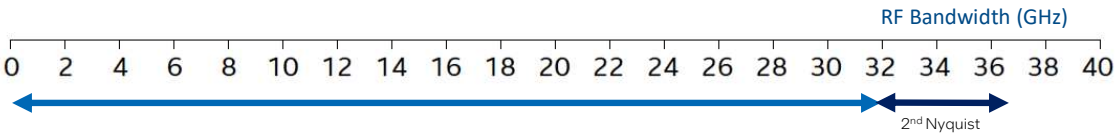


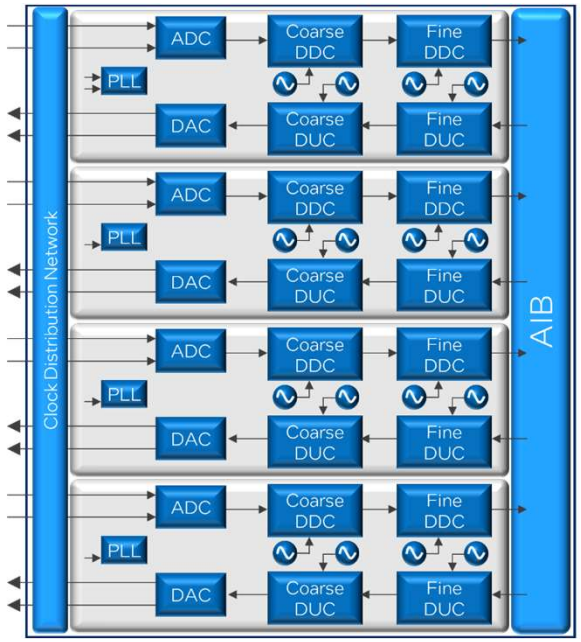


Up to 32 GHz of ADC/DAC RF

Wideband 64 GSPS Data Converter Tile (DCT) Overview

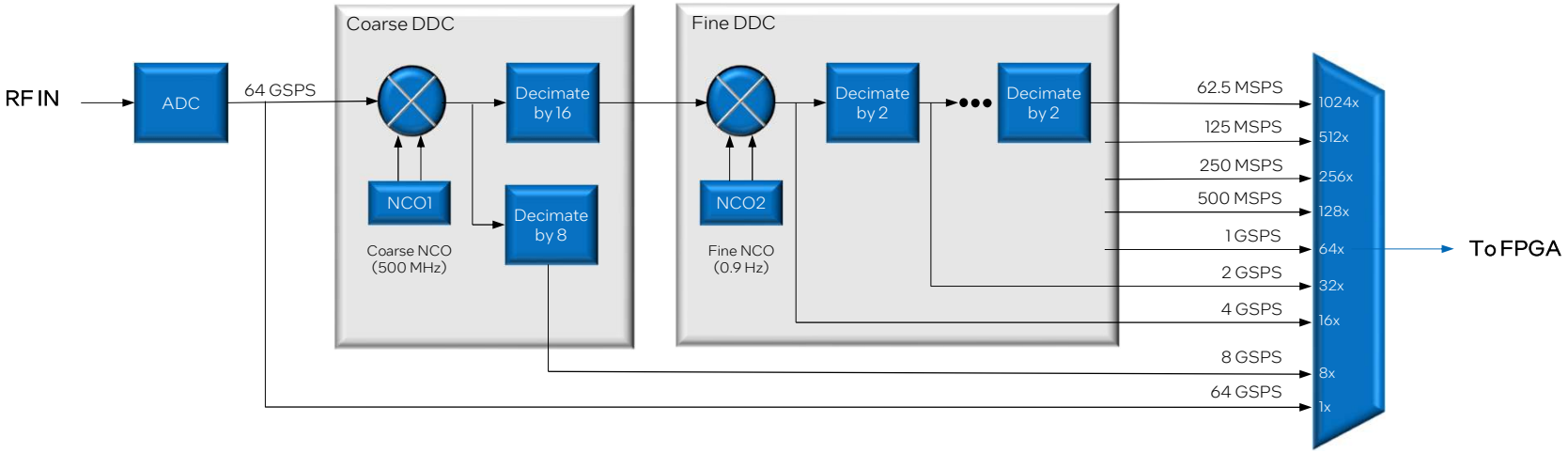
- On-die ADC / DAC compensation networks
  - No FPGA resources required
- Four parallel high speed control ports from FPGA
  - Fast control, custom calibration coefficient support
- Leverages open Advanced Interface Bus (AIB)
  - Standardized by CHIPs Alliance
- Reduces power and latency using AIB/EMIB
  - No SERDES or JESD204C protocol overhead
- Reduces size, integrates historically analog circuitry
  - Eliminates/reduces super heterodyne architectures



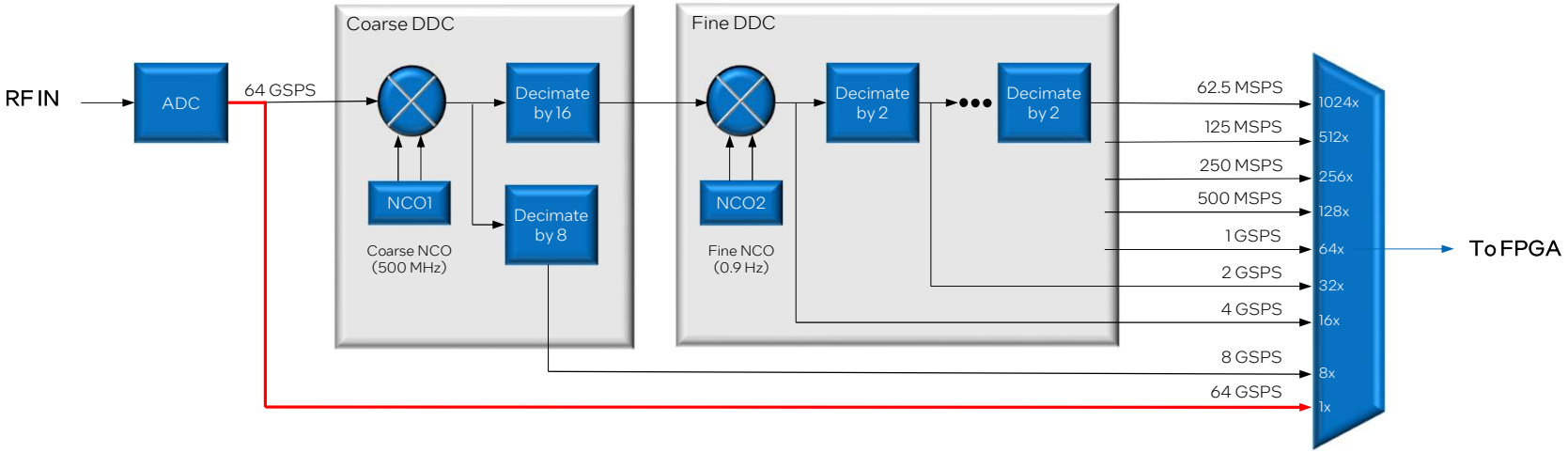


Up to 32 GHz of ADC/DAC RF

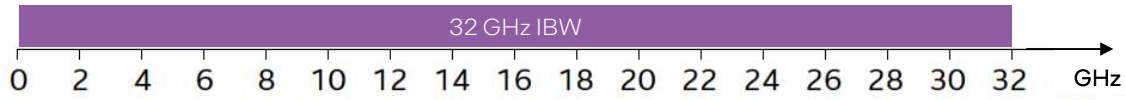
Wideband DCT RX Architecture



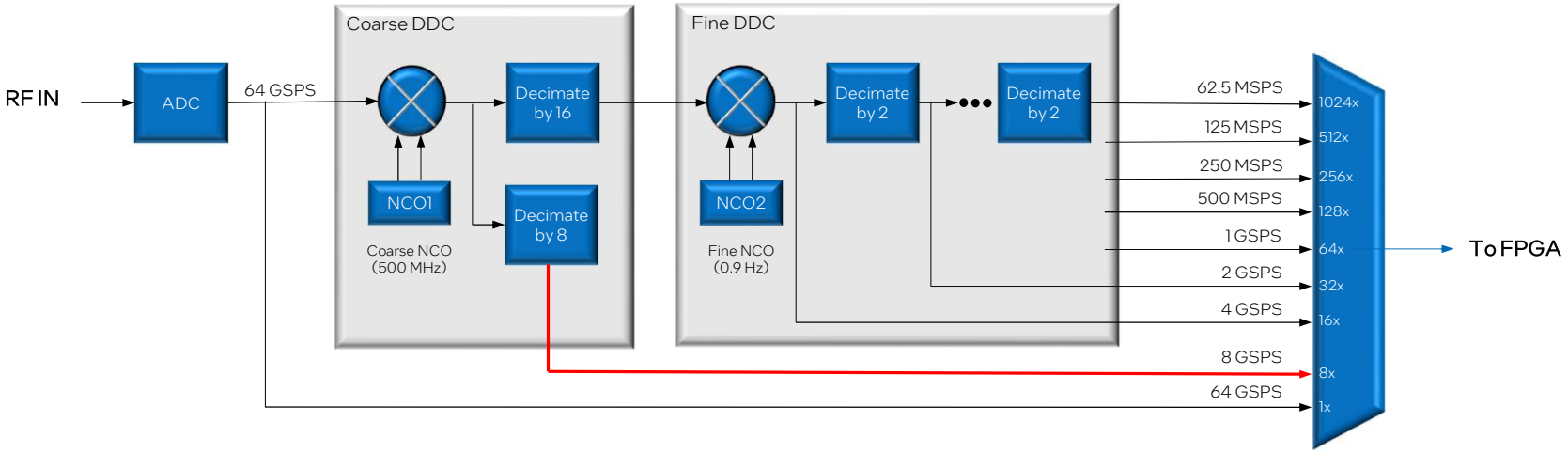
Wideband DCT RX Architecture: 1X Mode



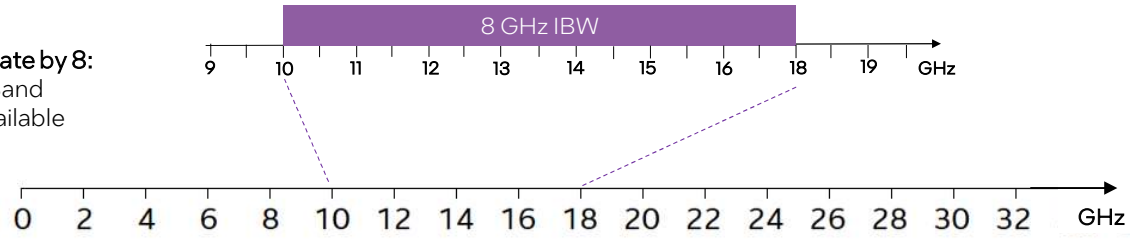
Wideband 1x Mode:
Full 32 GHz of IBW



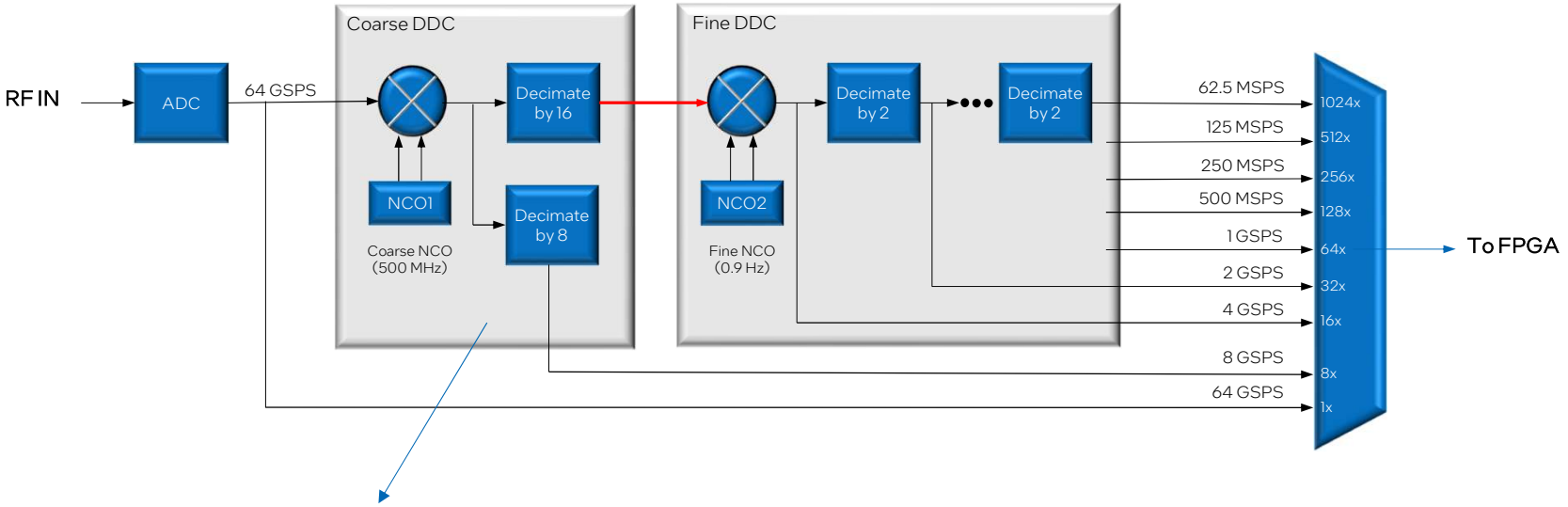
Wideband DCT RX Architecture: 8X Mode

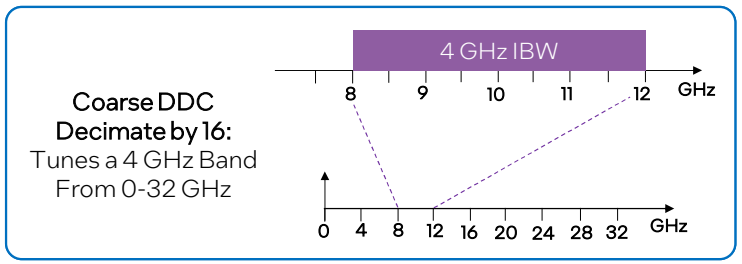


Coarse DDC Decimate by 8:
Tunes 8 GHz Band
From 32 GHz Available



Dual Stage DDC Operation: 16X and Above





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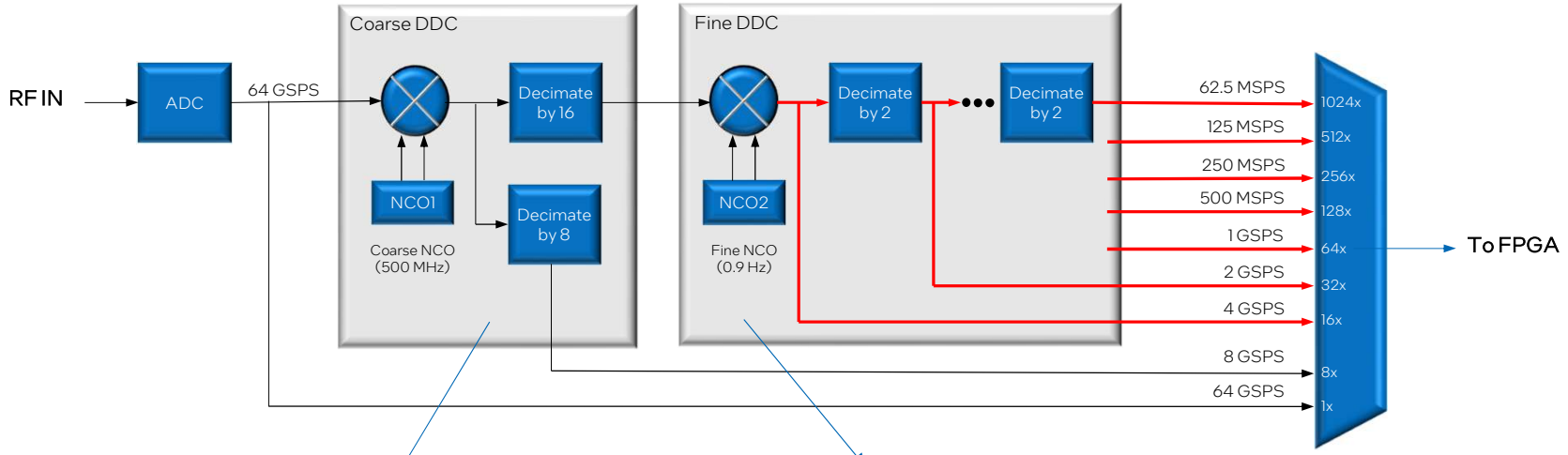
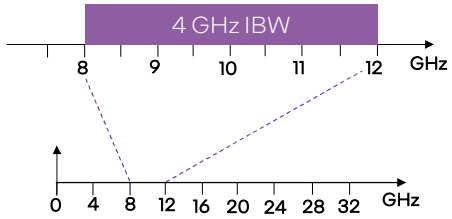
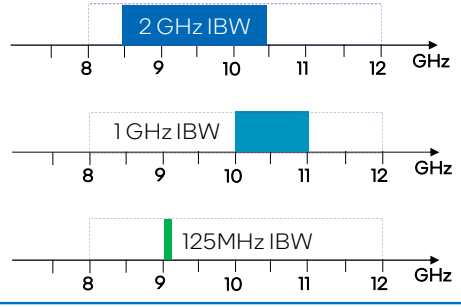


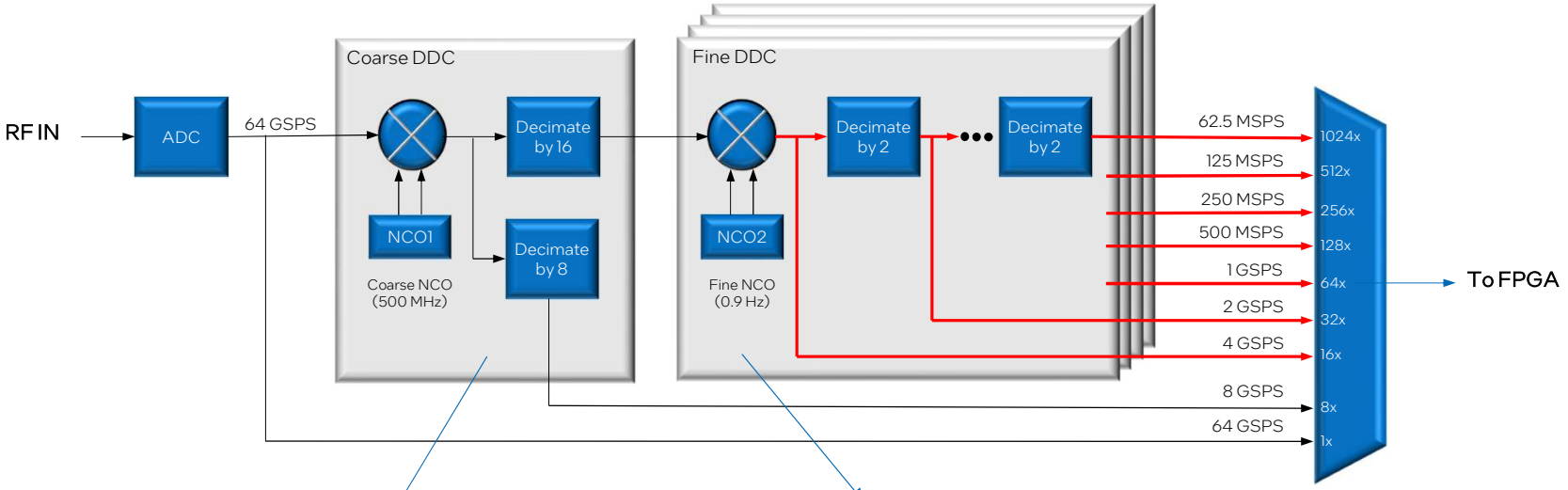
Coarse DDC Decimate by 16: Tunes a 4 GHz Band From 0-32 GHz



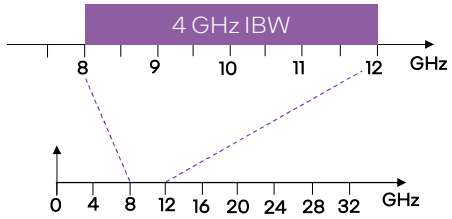


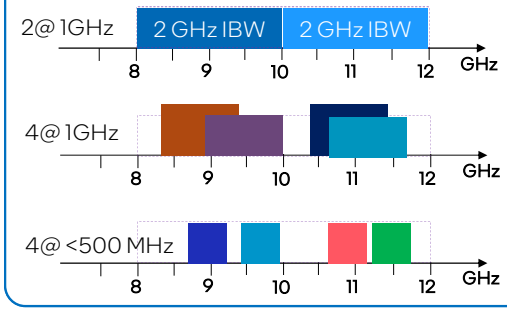
Fine DDC: "Zooms" in Within the 4 GHz Tuned Band From Coarse DDC

Dual Stage DDC Operation: Up to Four DDCs per ADC



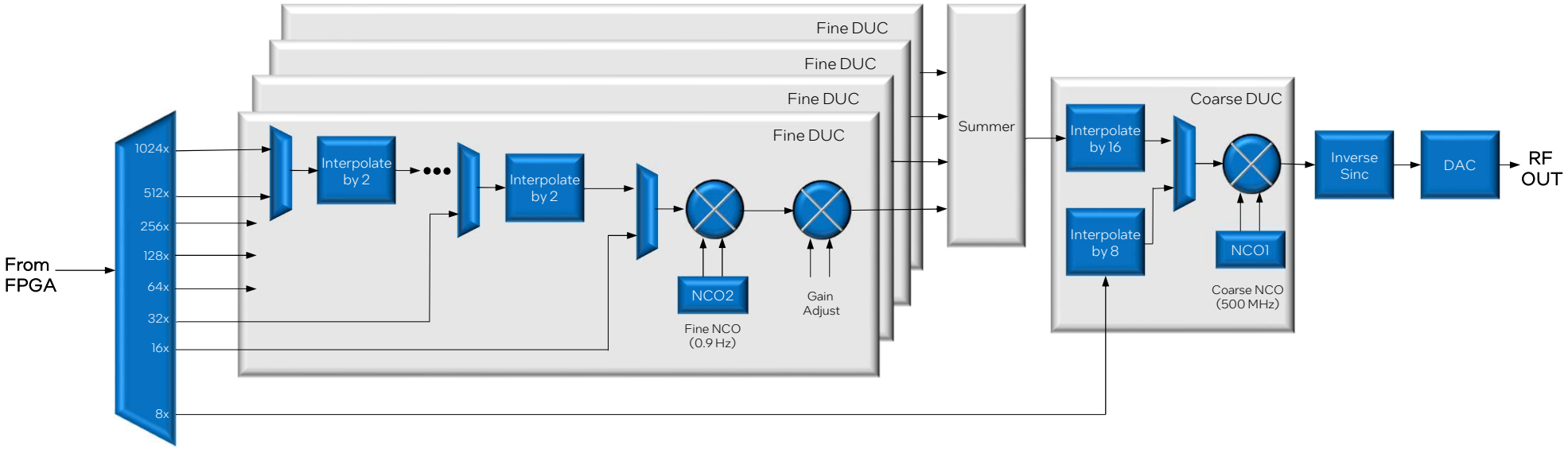
Coarse DDC Decimate by 16: Tunes a 4 GHz Band From 0-32 GHz





Fine DDCs: "Zoom" in Within the 4 GHz Tuned Band From Coarse DDC Up to Four Fine DDCs Available

Wideband DCT TX Architecture

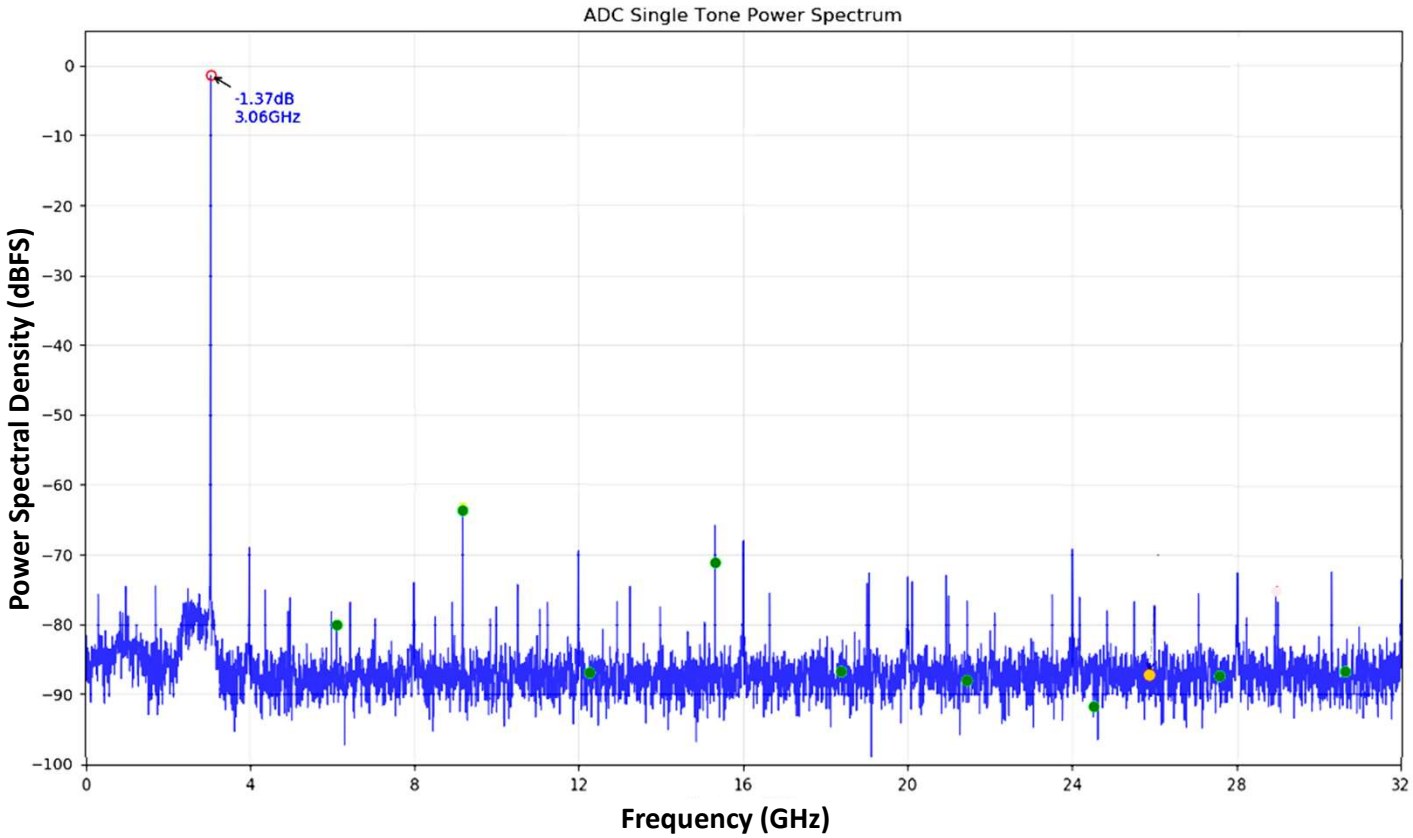


Wideband Data Converter Channels / Bandwidth Per Tile

Mode	Decimate / Interpolate Rate	Sample Rate (GSPS)	Max IBW (GHz)	Coarse DDC Per Port	Fine DDCs Per Port	Total Channels Per Tile
A[1,2]	x1	64	32	NA	NA	1
B	x8F[3]	8	8	1	NA	2
C	x8H[4]	8	8	1	NA	4
D	x16	4	4	1	1	4
E	x32	2	2	1	2	8
F	x64	1	1	1	4	16
G	x128	0.50	0.50	1	4	16
H	x256	0.25	0.25	1	4	16
I	x512	0.12	0.12	1	4	16
J	x1024	0.06	0.06	1	4	16

[1] Mode A available for ADC only
[2] Mode A represents real bandwidth, all other modes complex
[3] 16 bit I, 16-bit Q
[4] 8 bit I, 8-bit Q

Intel Agilex 9® AGRW014 FPGA Test Results: RX



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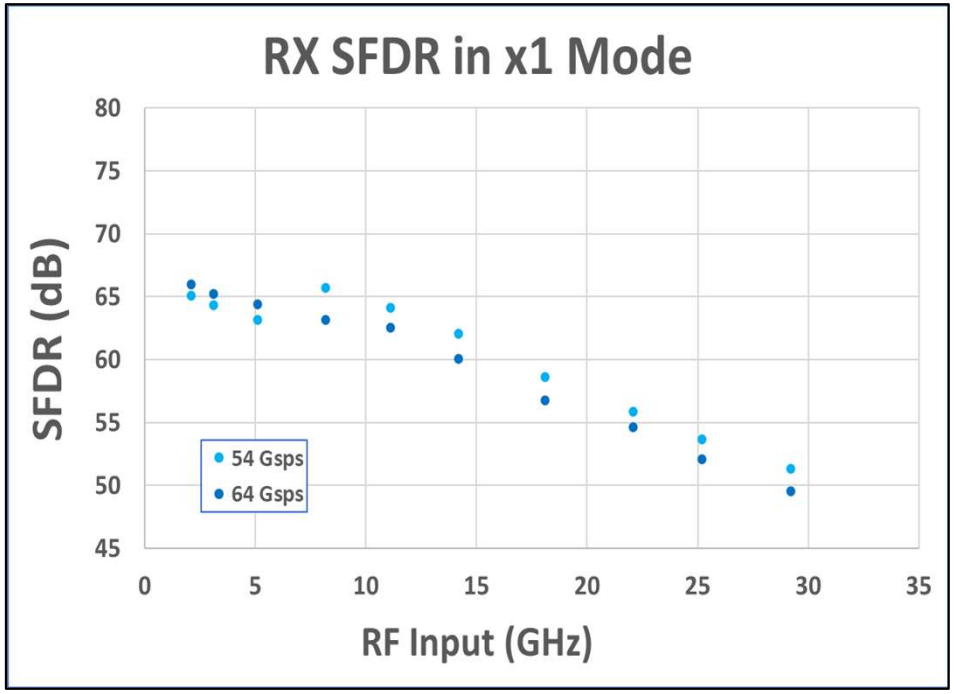

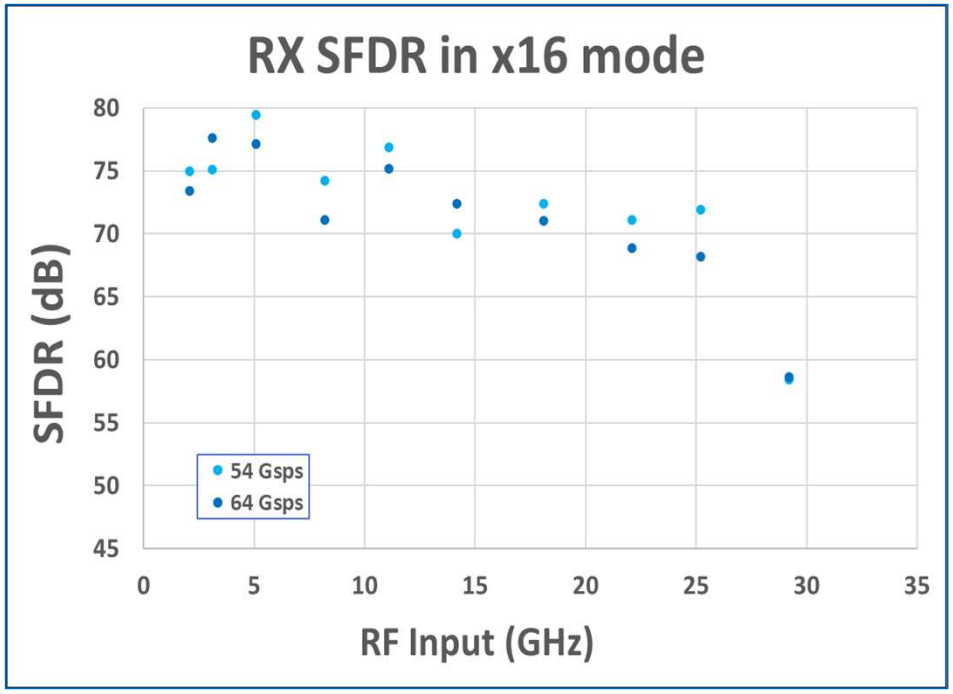

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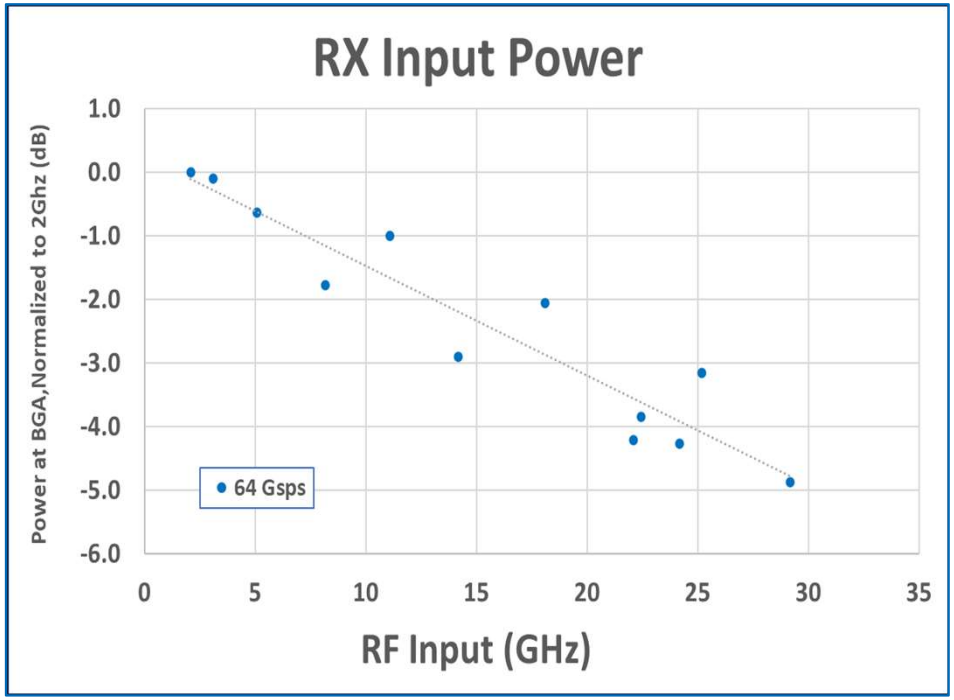
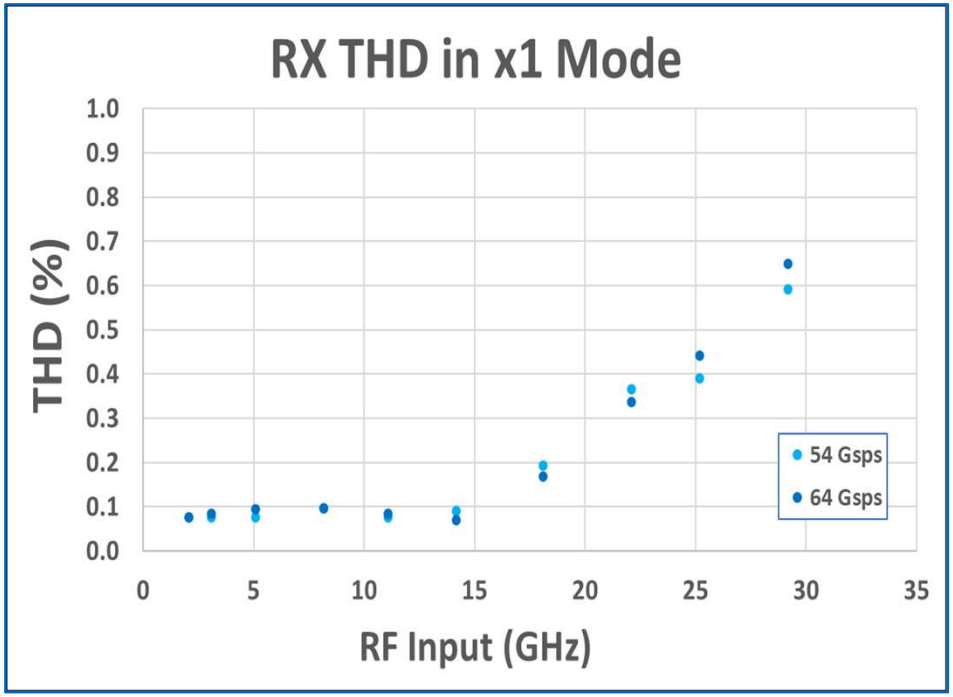
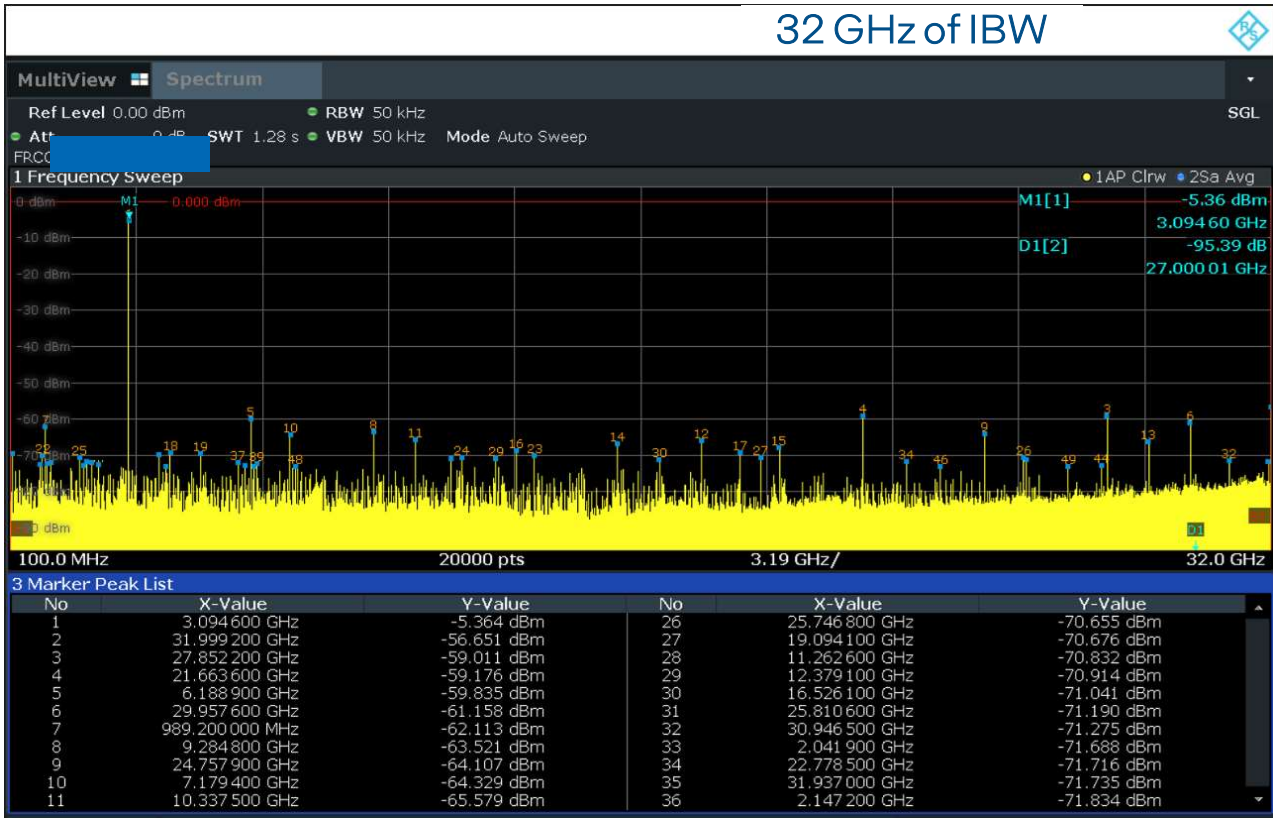


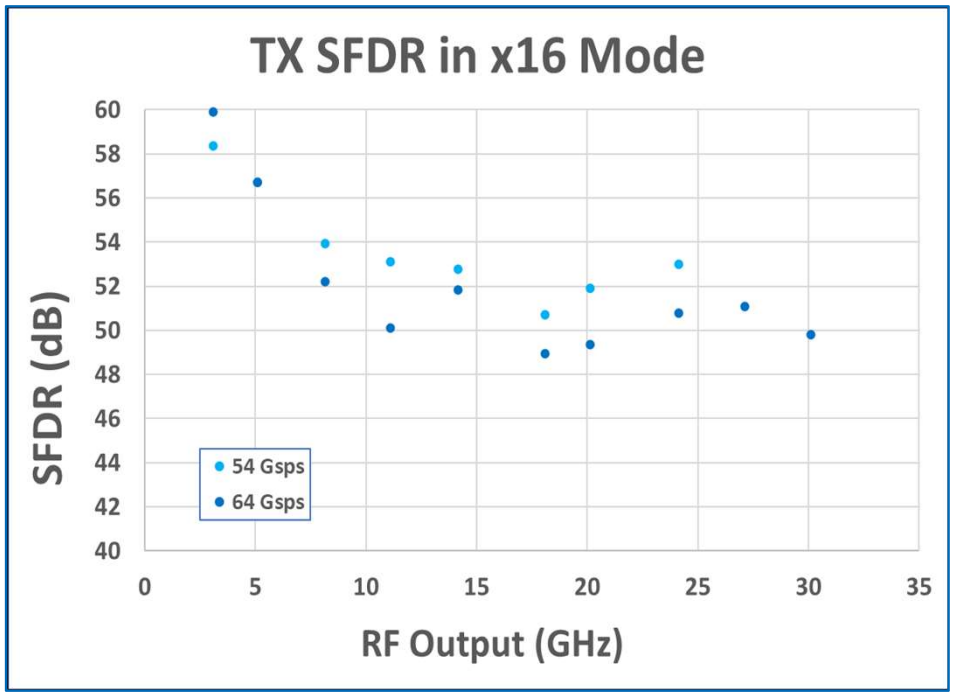


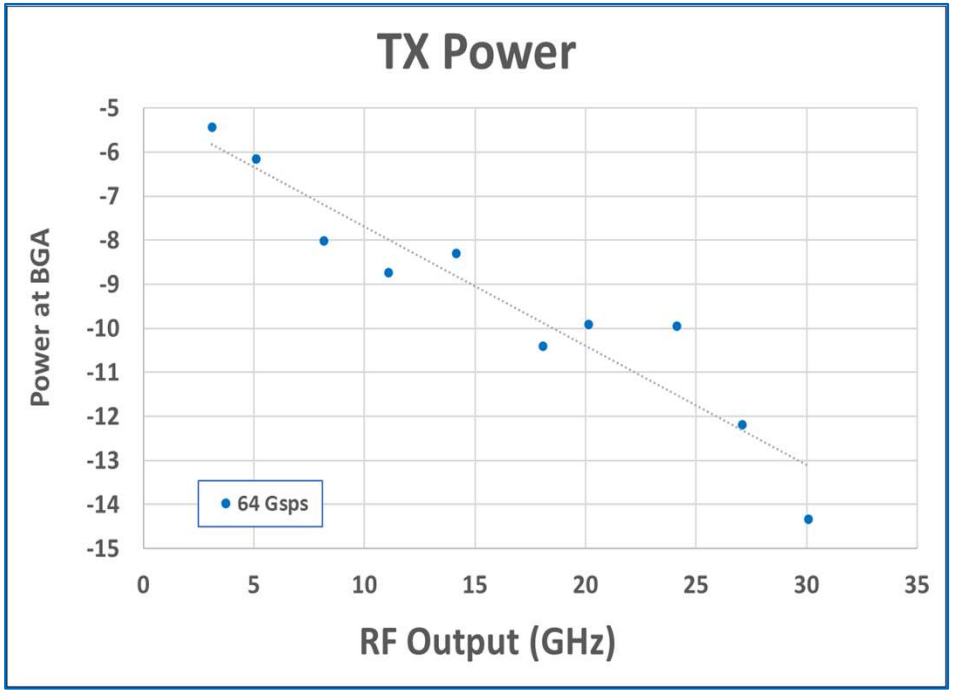
Intel Agilex 9® AGRW014 FPGA Test Results: TX



No	X-Value	Y-Value	No	X-Value	Y-Value
1	3.094 600 GHz	-5.364 dBm	26	25.746 800 GHz	-70.655 dBm
2	31.999 200 GHz	-56.651 dBm	27	19.094 100 GHz	-70.676 dBm
3	27.852 200 GHz	-59.011 dBm	28	11.262 600 GHz	-70.832 dBm
4	21.663 600 GHz	-59.176 dBm	29	12.379 100 GHz	-70.914 dBm
5	6.188 900 GHz	-59.835 dBm	30	16.526 100 GHz	-71.041 dBm
6	29.957 600 GHz	-61.158 dBm	31	25.810 600 GHz	-71.190 dBm
7	989.200 000 MHz	-62.113 dBm	32	30.946 500 GHz	-71.275 dBm
8	9.284 800 GHz	-63.521 dBm	33	2.041 900 GHz	-71.688 dBm
9	24.757 900 GHz	-64.107 dBm	34	22.778 500 GHz	-71.716 dBm
10	7.179 400 GHz	-64.329 dBm	35	31.937 000 GHz	-71.735 dBm
11	10.337 500 GHz	-65.579 dBm	36	2.147 200 GHz	-71.834 dBm

Intel Agilex 9® AGRW014 FPGA Test Results: TX





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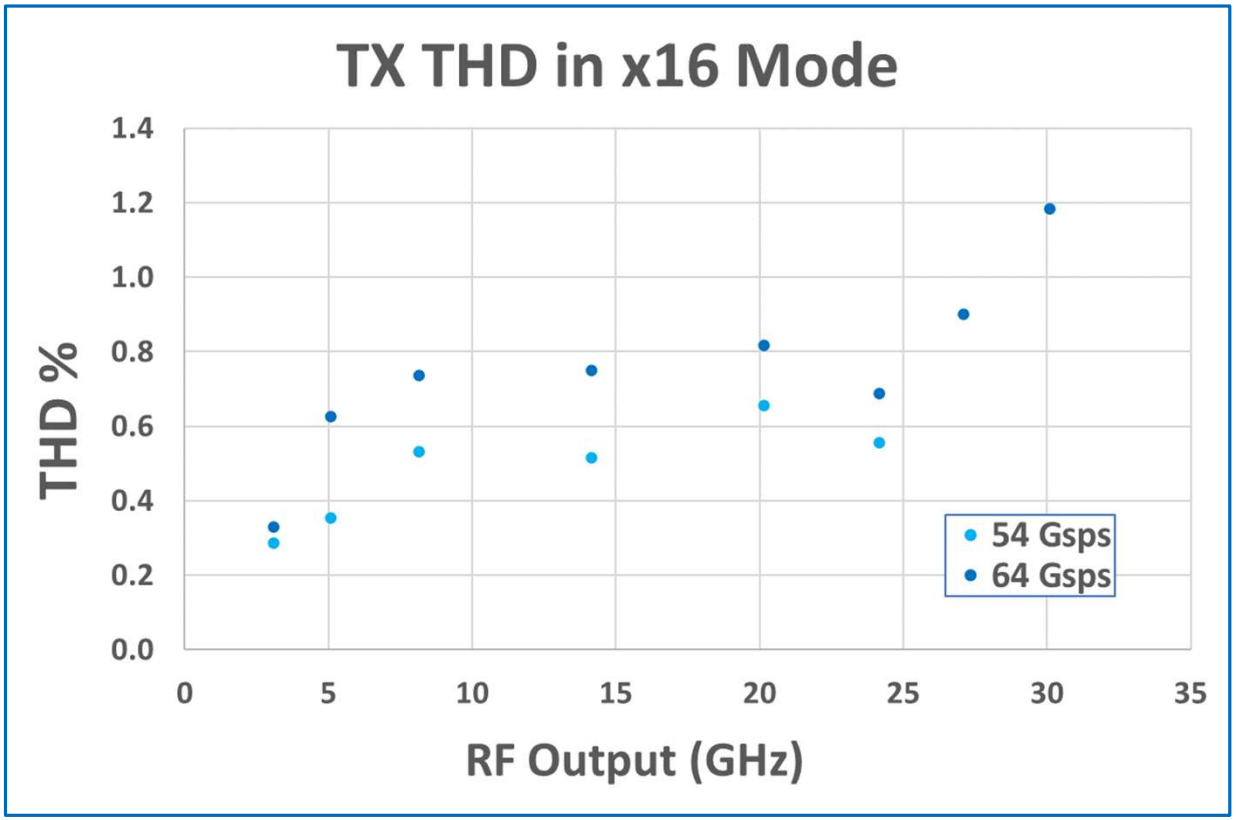
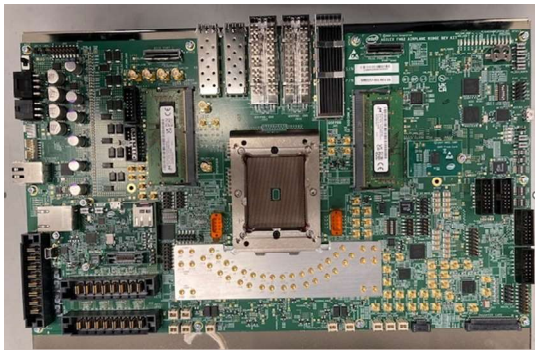


Intel® 64 GSPS Direct RF-Series FPGA Development Kits

- Development kits to be available for each Intel Agilex® Direct RF FPGA devices
- All RF ports available for test
- On board clocking or connectors to support external clocking schemes
- On board DDR memory for algorithm development
- FPGAs includes Quad ARM-A53 hard processor subsystem for embedded control
- High speed transceivers support PCIe and Ethernet backhaul

AGWR014 Development Kit

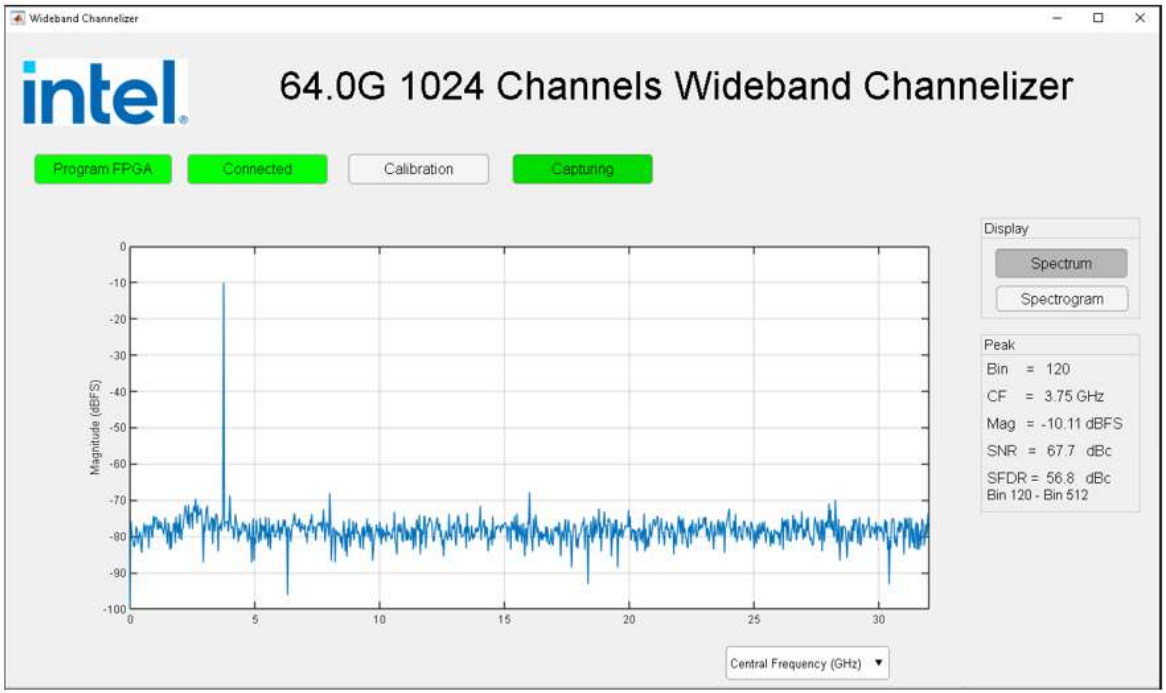


AGWR027 Development Kit

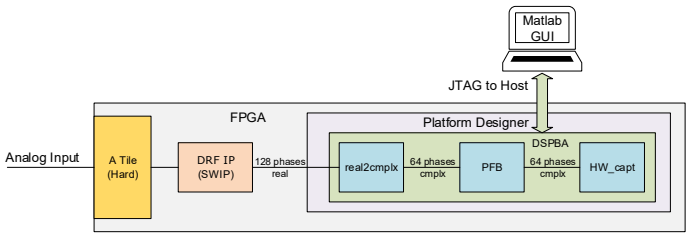
Intel® Direct RF Development Tools

- Direct RF Design Suite
  - Playback and capture for RF evaluation
  - Wideband 32 GHz channelizer
  - Wideband agility
  - Multi-device phase synchronization
  - Time delay beamforming
  - Other designs also under development
  - All use DSP Builder Advanced Blockset (Intel's Matlab® Simulink® Blockset)
- Direct RF Evaluation Platform
  - Matlab® script-based test environment
- Other Tools
  - Latency calculator, Spur calculator

Intel® Direct RF Design Suite: Wideband Channelizer

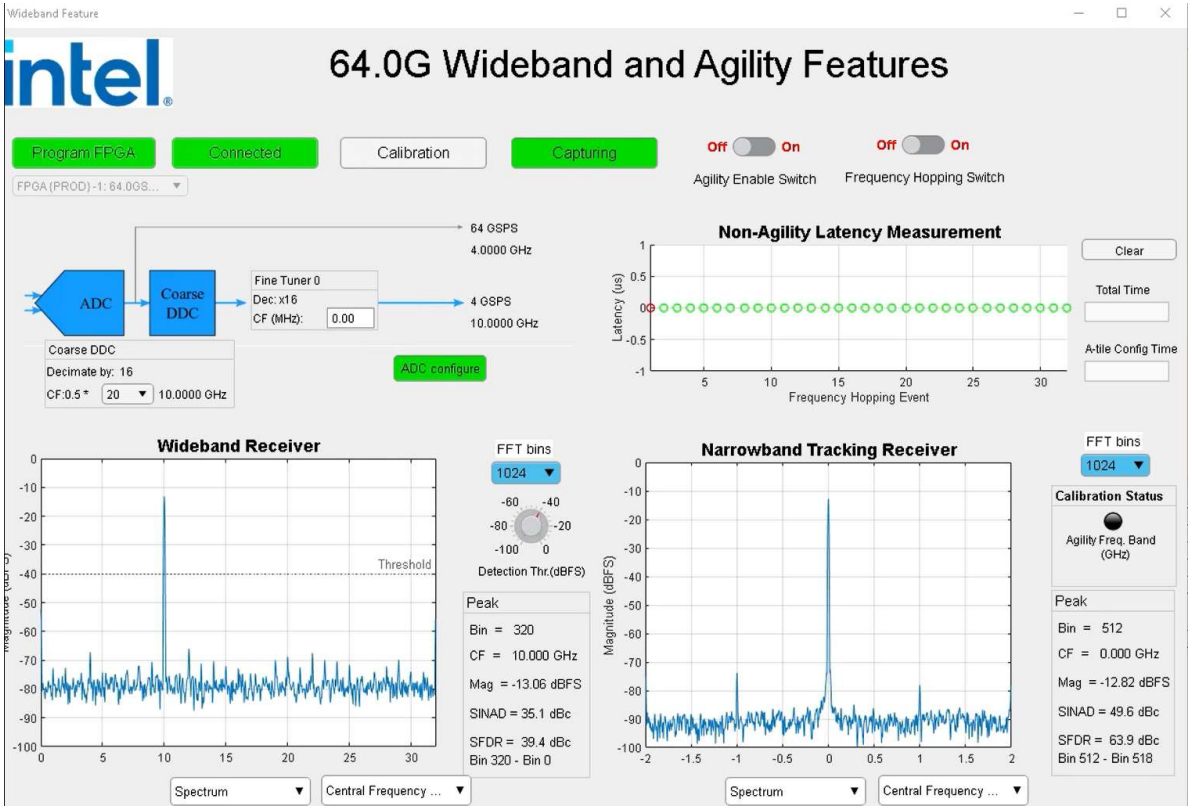


- 64 Gsps ADC sampling
- 32 GHz of IBW
- Single Channel ADC
- Matlab Simulink DSP Builder Design Flow



Supports Variable 64-1024 channels in real time

Intel® Direct RF Design Suite: Wideband Agility

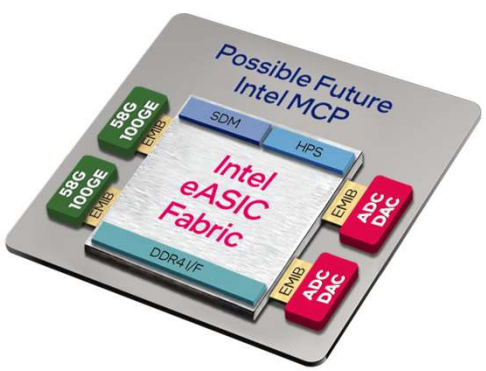


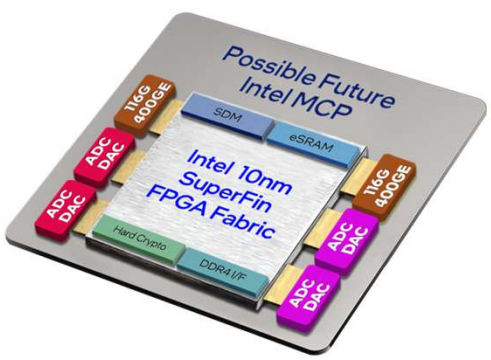
- Wideband Receiver ("Sniffer")
  - Tile 0 operating at x1, 32 GHz
- Narrowband Tracking Receiver
  - Tile 1 operating at x16, 4 GHz
- Wideband Receiver Threshold value sets tuner for Narrowband Tracking Receiver
- Optimized coefficients move with frequency tuning
- Matlab Simulink DSP Builder Design Flow

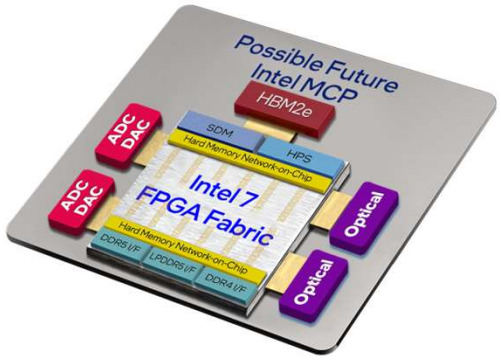
Possible Future Heterogeneously Integrated MCPs

Chip to Chip Interface

AIB over EMIB

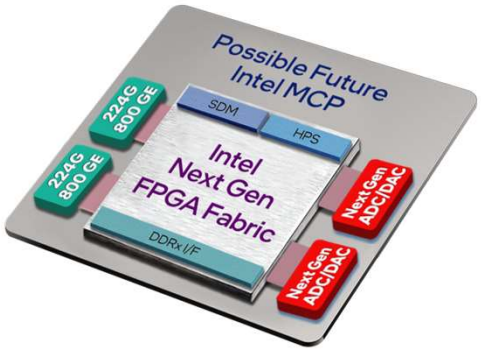


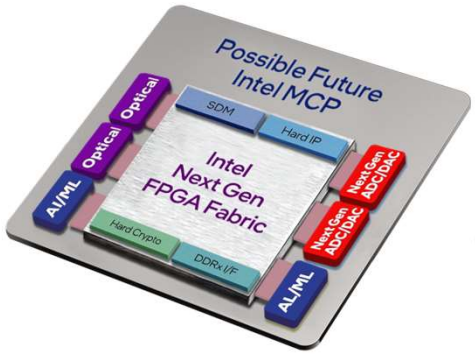


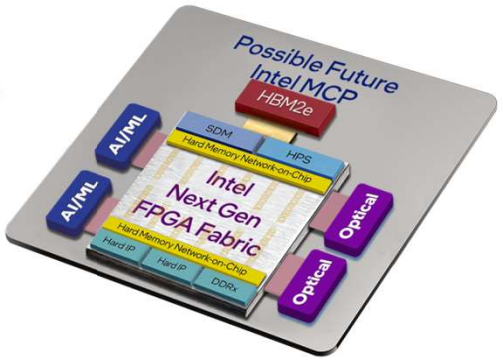


Chip to Chip Interface

UCIe-Standard
UCIe-Advanced

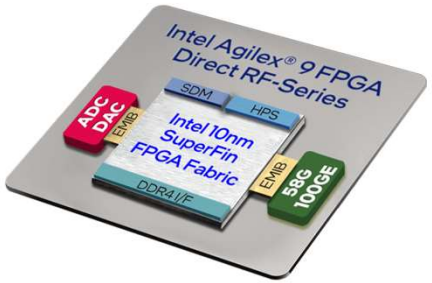


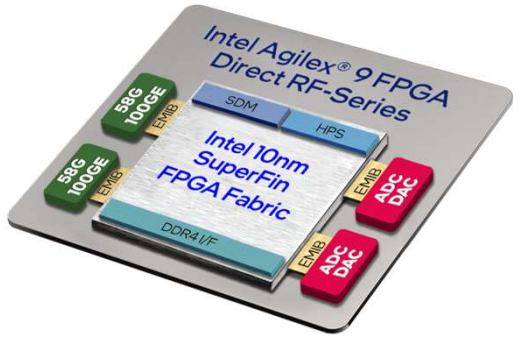




Wideband Intel Agilex® 9 Direct RF-Series FPGA Summary

- Leverage Intel's heterogeneously integrated FPGAs methodology using EMIB and AIB PHY
- Unprecedented combination of channel count and frequency agility in a small form factor MCP
- Significantly reduces Size, Weight, Power and Cost
- 32 GHz of ADC IBW for processing in FPGA (x1 Mode)
- Up to thirty-two 1 GHz TX/RX channels available for diverse spectrum requirements
- Reference designs, tools and Direct RF FPGA evaluation boards available to jumpstart development





Details on Intel Agilex® FPGA Performance, Power and Software Support Numbers

- Up to 40% Higher Performance Compared to Intel Stratix 10 FPGAs
- Derived from benchmarking an example design suite comparing maximum clock speed (Fmax) achieved in Intel Stratix 10 devices with the Fmax achieved in Intel Agilex devices, using Intel Quartus Prime Software. On average, designs running in the -2 speed grade of Intel Agilex FPGAs achieve a 50% improvement in Fmax compared to the same designs running in the most popular speed grade of Stratix 10 devices (-2 speed grade), tested June 2020.
- Up to 40% Lower Total Power Compared to Intel Stratix 10 FPGAs
- Derived from benchmarking an example design suite comparing total power estimates of each design running in Intel Stratix 10 FPGAs compared to the total power consumed by the same design running in Intel Agilex FPGAs. Power estimates of Intel Stratix 10 FPGA designs are obtained from Intel Stratix 10 Early Power Estimator; power estimates for Intel Agilex FPGA designs are obtained using internal Intel analysis and architecture simulation and modeling, tested February 2019.
- Up to 40 TFLOPs of DSP Performance (FP16 Configuration)
- Each Intel Agilex DSP block can perform two FP16 floating-point operations (FLOPs) per clock cycle. Total FLOPs for FP16 configuration is derived by multiplying 2x the maximum number of DSP blocks to be offered in a single Intel Agilex FPGA by the maximum clock frequency that will be specified for that block.
- 30% Improvement in Compile Times / 15% Improvement in Memory Utilization
- Comparison is made between Intel Quartus Prime Software 18.1 and Intel Quartus Prime 19.1. Derived from benchmarking an example design suite comparing compile times and memory utilization for designs in Intel Quartus Prime Software 18.1 with compile times and memory utilization for same designs in Intel Quartus Prime Software 19.1, tested February 2019.

Legal Notices and Disclaimers – Part 1

Performance varies by use, configuration and other factors. Learn more at www.Intel.com/PerformanceIndex.

Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.

Your costs and results may vary.

Intel technologies may require enabled hardware, software or service activation.

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1. Intel Agilex 7 FPGAs M-Series theoretical maximum bandwidth of 1.099 TBps with 2 banks of HBM2e using ECC as data and 8 DDR5 DIMMs as compared to Xilinx Versal HBM memory bandwidth of 1.056 TBps from https://www.xilinx.com/products/silicon-devices/acap/versal-hbm.html#productAdvantages and from https://www.xilinx.com/content/dam/xilinx/support/documentation/selection-guides/versal-hbm-product-selection-guide.pdf as of October 14, 2021 and to Achronix Speedster 7t memory bandwidth of 0.5 TBps from https://www.achronix.com/sites/default/files/docs/Speedster7t_Product_Brief_PB033.pdf as of October 14th 2021

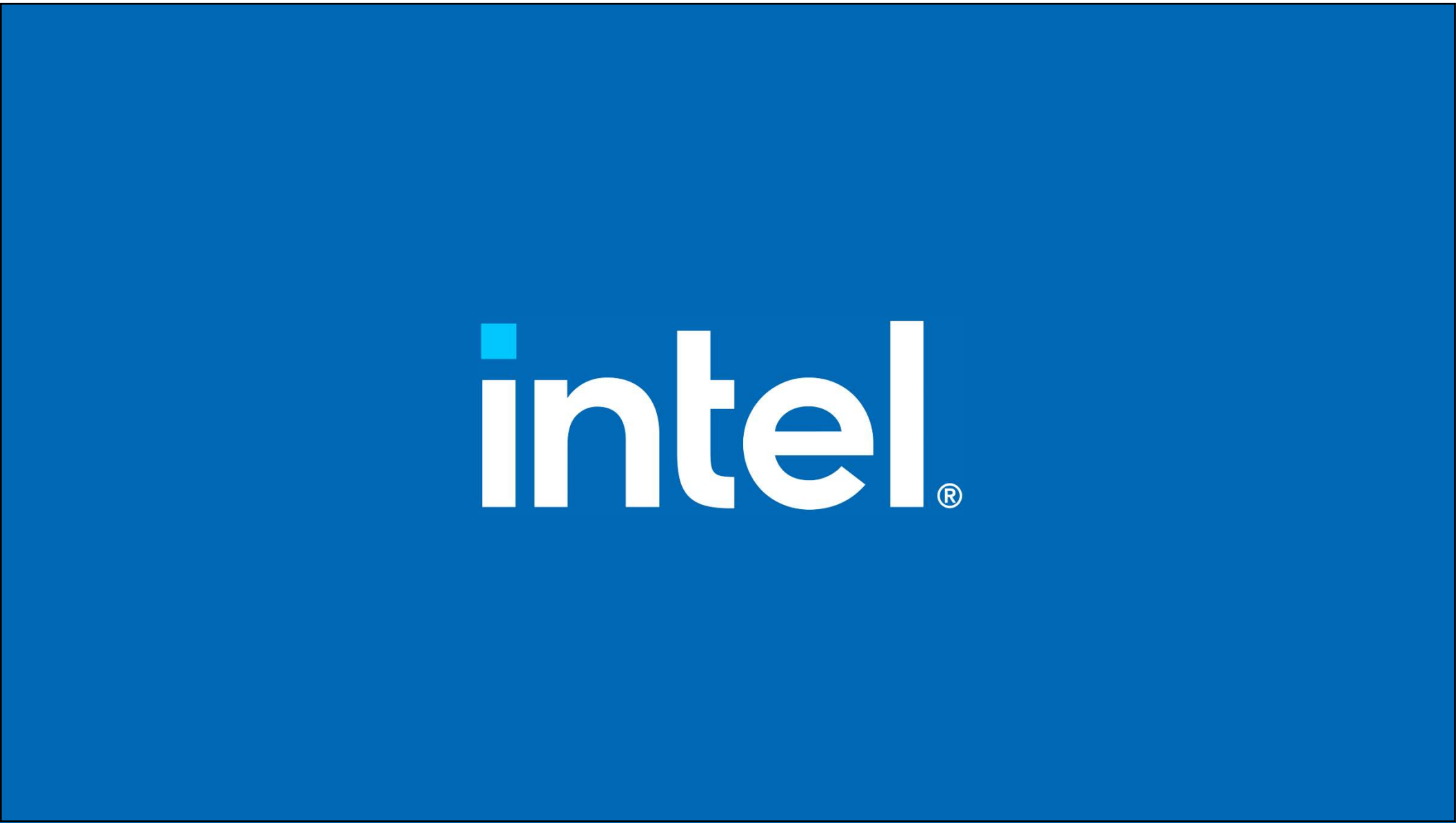
2. Intel Agilex 7 FPGAs M-Series with HBM2e, 700 MHz maximum clock frequency for hard memory NoC initiator (user logic AXI4 port connects to initiator AXI4 port to initiate memory requests on the NoC). Intel Stratix 10 MX with HBM2, 405 MHz for equivalent HBM2 switch function in -1 speed grade. Ratio of clock frequency is 700 MHz/405 MHz = 1.7, Intel Agilex 7 FPGAs M-Series offers a 1.7x improvement in performance in HBM throughput compared to prior generation Intel Stratix 10 MX.

3. Intel Agilex 7 FPGAs M-Series DSP compute density projected at 88.6 INT8 TOPs and 18.45 FP32 TFLOPs, compared to Xilinx Versal HBM at 74.9 INT8 TOPs and 17.5 FP32 TFLOPs from https://www.xilinx.com/content/dam/xilinx/support/documentation/selection-guides/versal-hbm-product-selection-guide.pdf as of October 14, 2021 and to Achronix Speedster 7t at 61.4 INT8 TFLOPs and no support for FP32, from https://www.achronix.com/machine-learning-processor as of October 14, 2021.

4. M-Series over 2x fabric performance/W results are based on projections of M-Series AGM039-R36B compared to measurements on I-Series AGI027-R31B, and power comparison of F-Series AGF014-2 to a Xilinx Versal FPGA fabric of equivalent density, where AGI027-R31B is projected to have the same core fabric performance/watt as measured on AGF014-2. Comparison assumes Xilinx Versal HBM has the same core fabric as similar Versal devices without HBM as of October 2021.

5. DDR4 max throughput of 3200 MT/s according to JEDEC at https://www.jedec.org/sites/default/files/docs/JESD79-4.pdf as of October 14, 2021. LPDDR4 max throughput of 4267 MT/s according to JEDEC at https://www.jedec.org/news/pressreleases/jedec-releases-lpddr4-standard-low-power-memory-devices as of October 14, 2021. M-Series DDR5 and LPDDR5 throughput projected at 5600 MT/s and 5500 MT/s respectively. Stratix 10 DDR4 throughput maximum at 2667 MT/s.

6. Intel Agilex 7 FPGAs M-Series compute density is projected at 18.45 FP32 TFLOPs, HBM2e memory bandwidth is projected at 410 GBps per stack, and EMIF DDR5 performance projected at 5600 MT/s. Prior generation Stratix 10 MX compute density is 6.3 FP32 TFLOPs, HBM2 memory bandwidth is 256 GBps per stack, and EMIF DDR4 performance is 2667 MT/s.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