SiFive

P870 High-Performance RISC-V Processor

HOT CHIPS 2023

RISC-V is based on standards

Standards Accelerate Software Adoption and Portability

Standards reduce cost

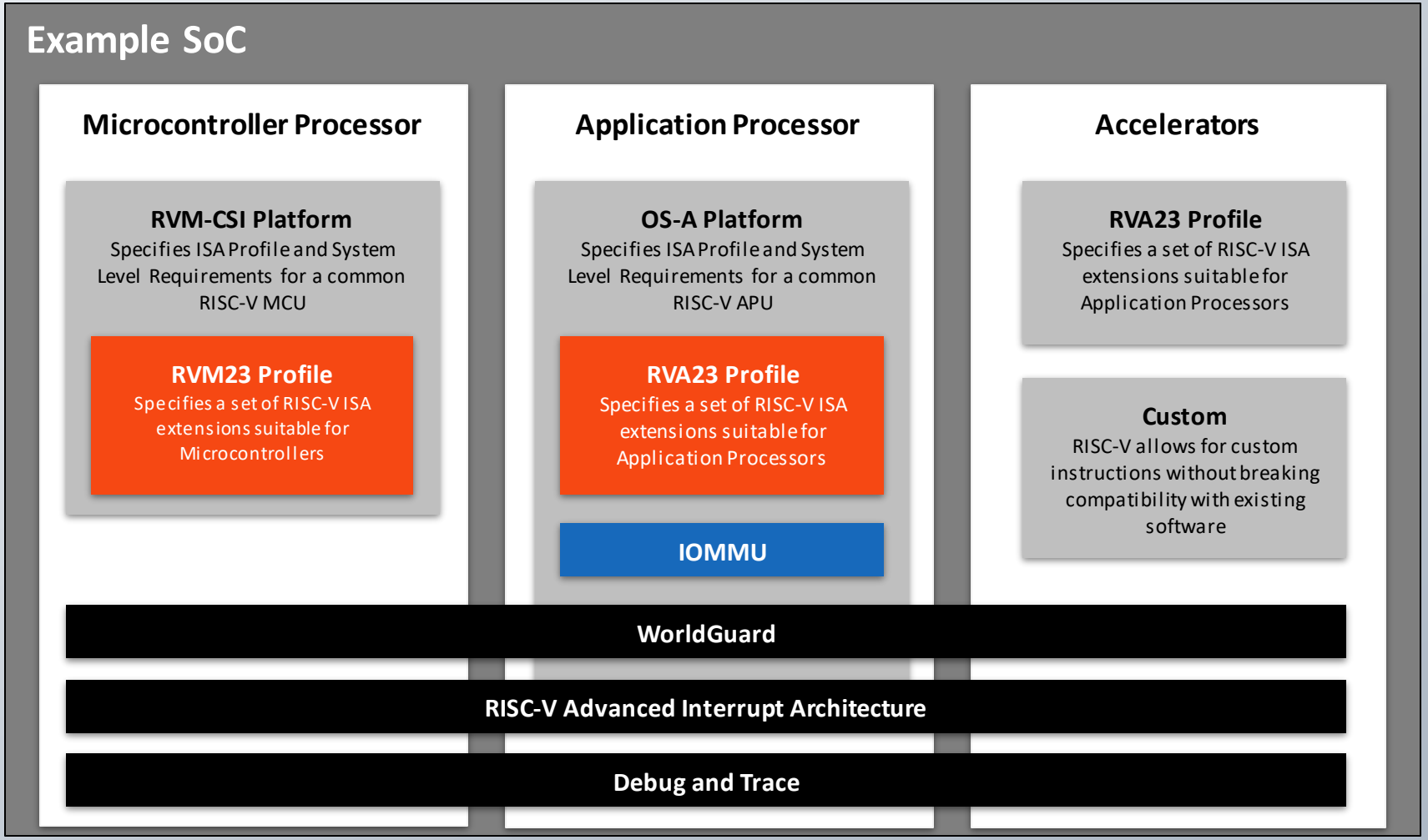
- Faster Adoption
- Compatibility across vendors

Layered standards enable customization

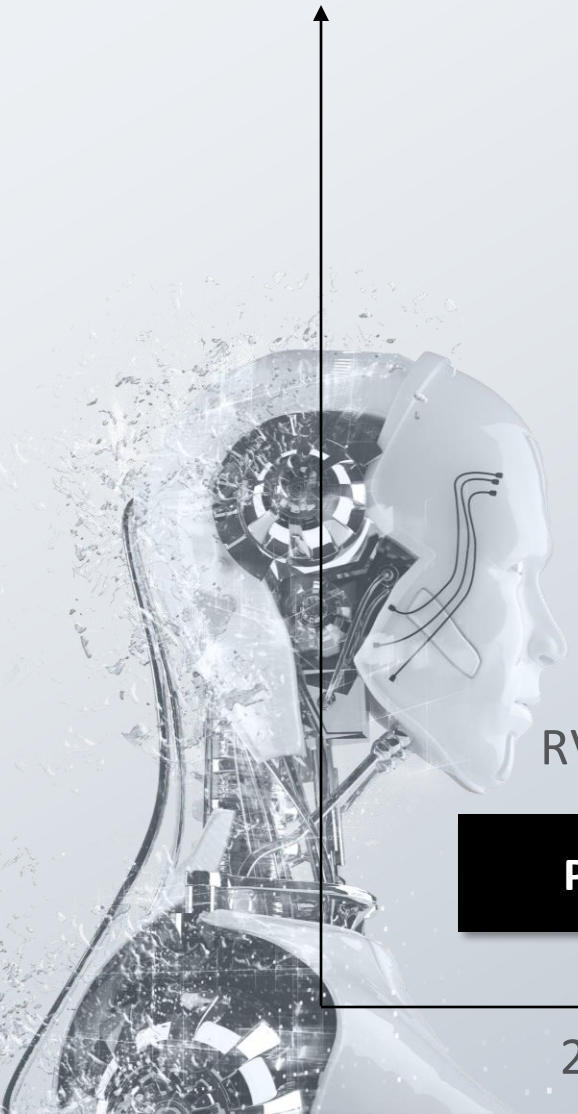
- RISC-V embraces customization without breaking compatibility

More than just ISA Standards

- RISC-V Standards extend beyond the Core ISA to system-level components



SiFive Performance family relentless innovation



RVA20+

P550

RVA22/RVA23

P650/P670

P450/P470

RVA23

P870

More performance
Higher core count
Leading RISC-V feature deployment

P870-A

Automotive specific features

3rd generation OoO core

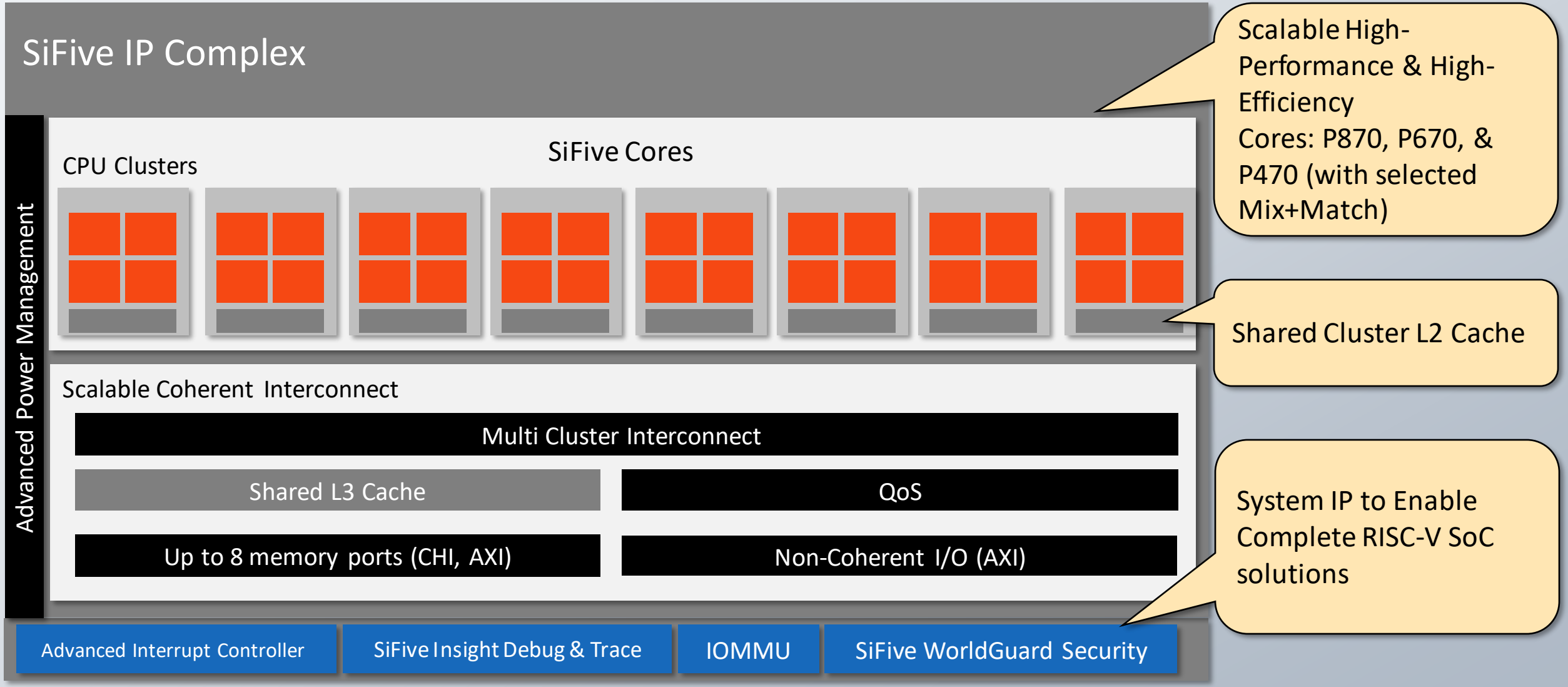
Customer In-Silicon Dates

2022

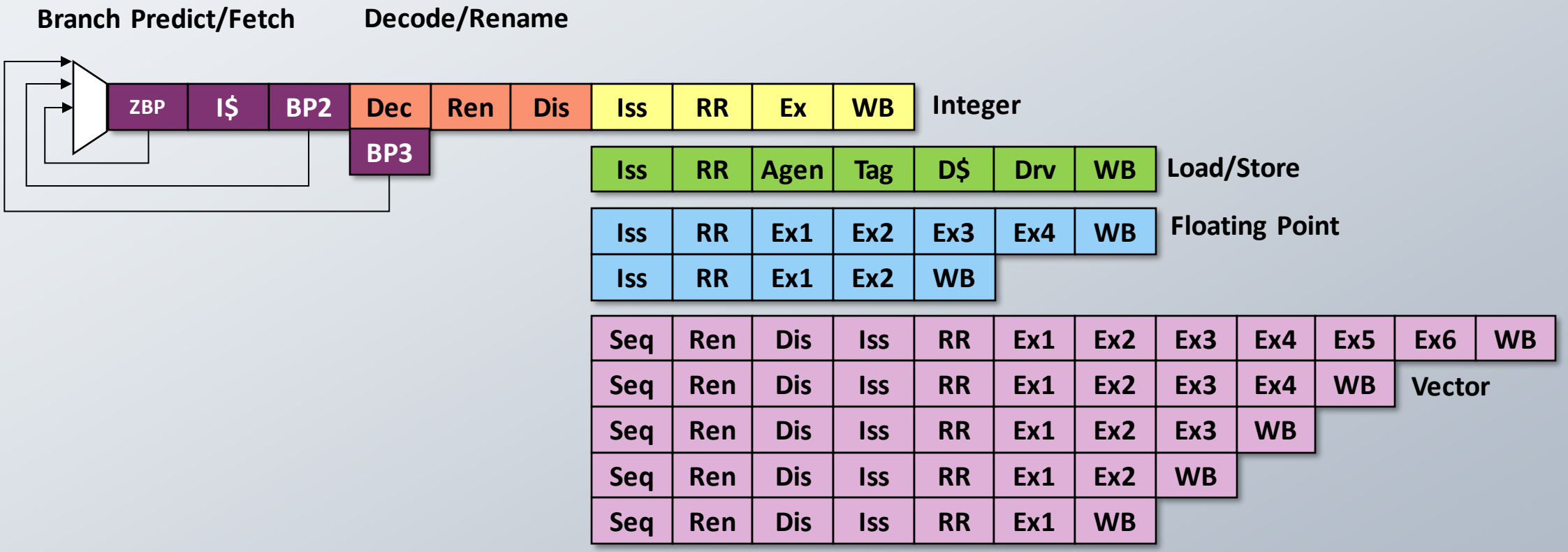
2023

2024

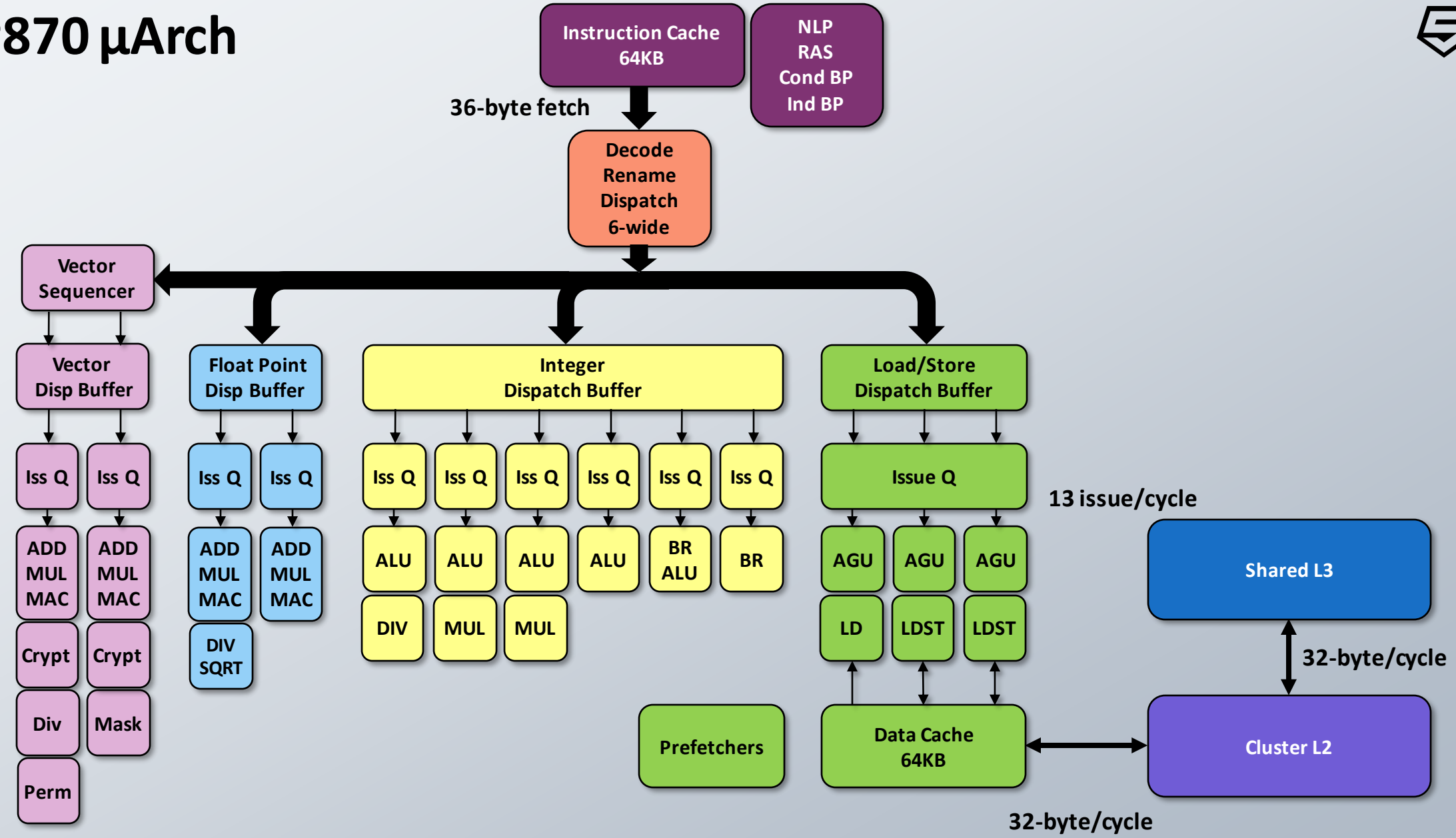
SiFive Provides Complete & Scalable Solutions



P870 Pipeline



P870 µArch



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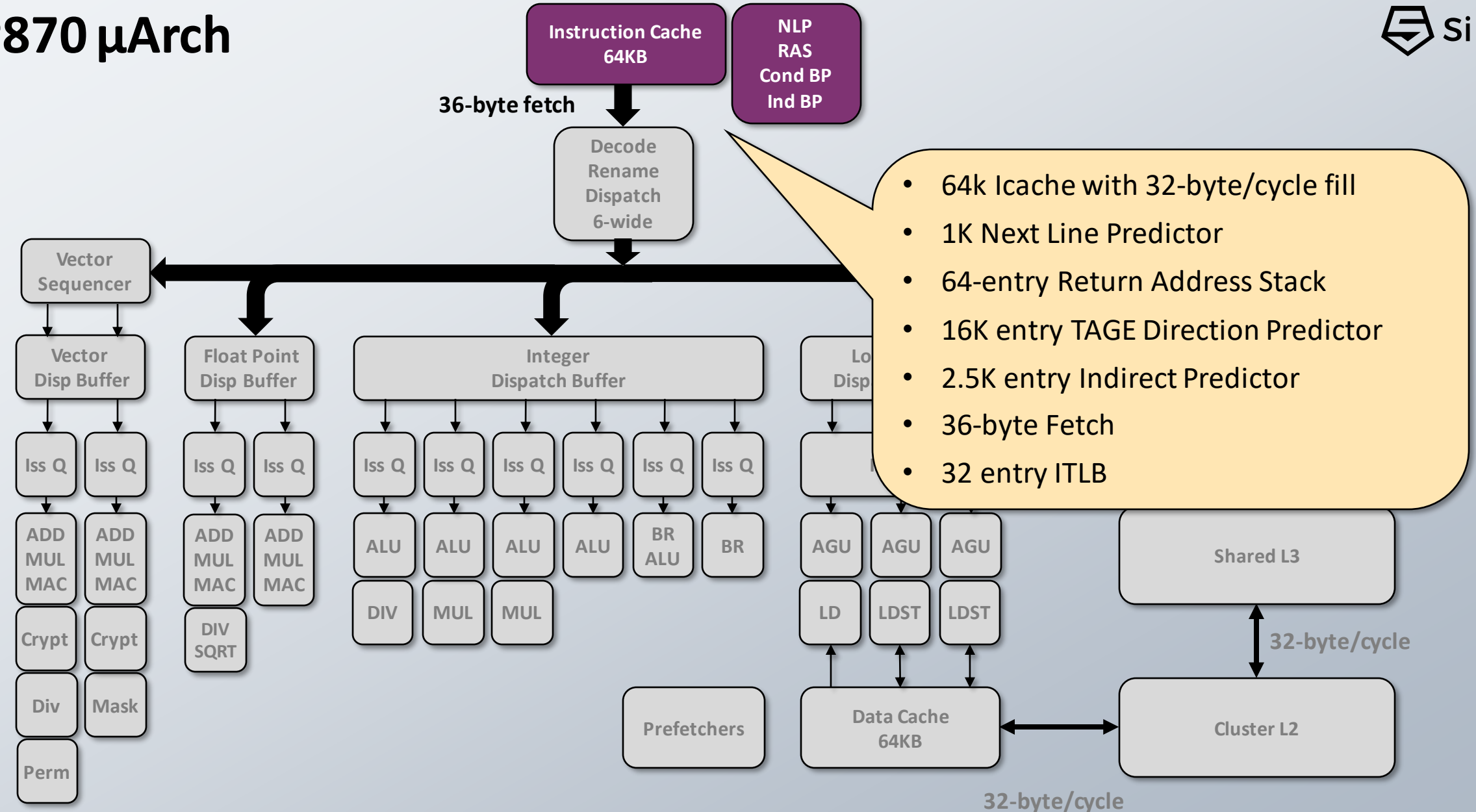
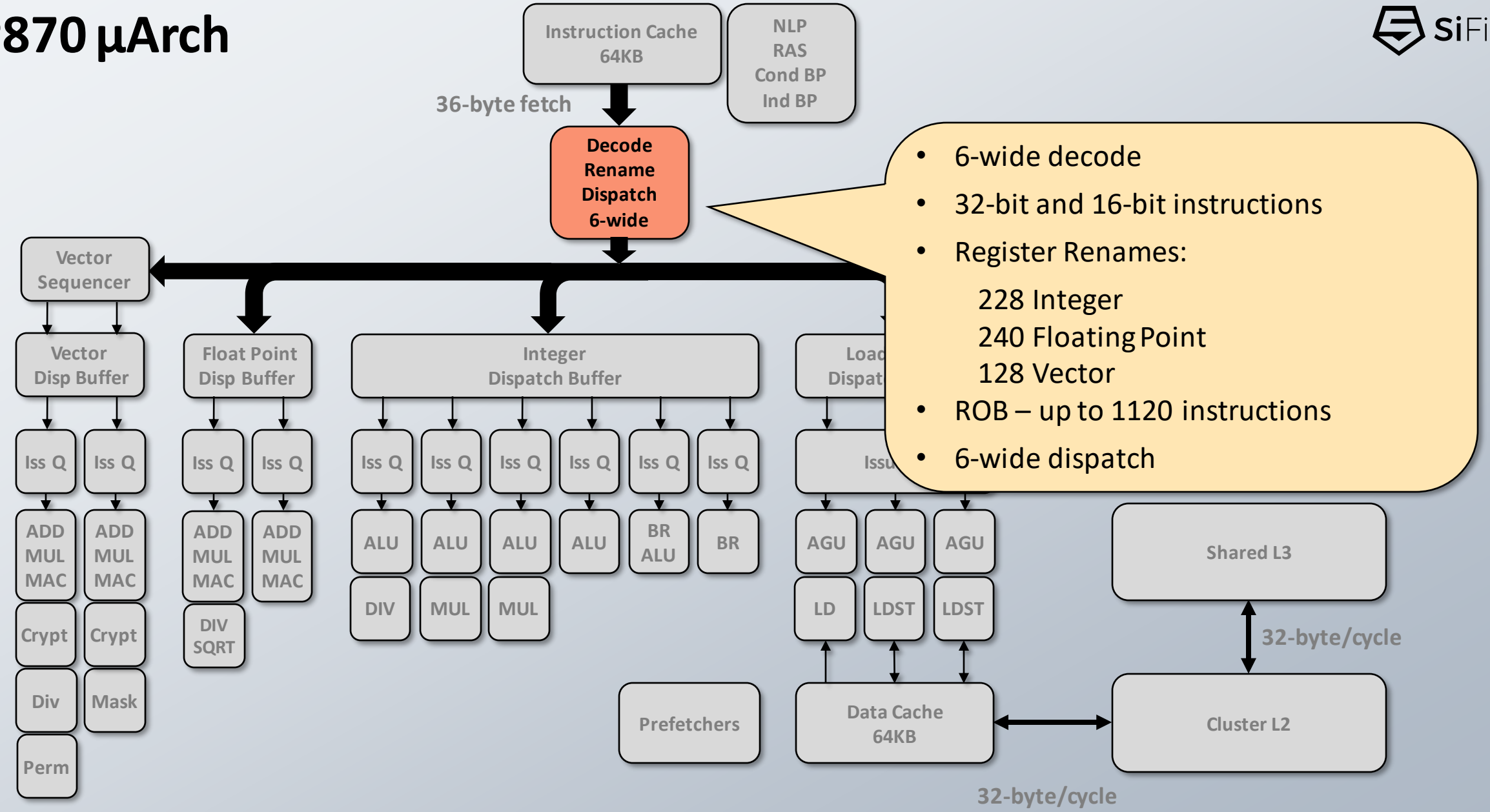
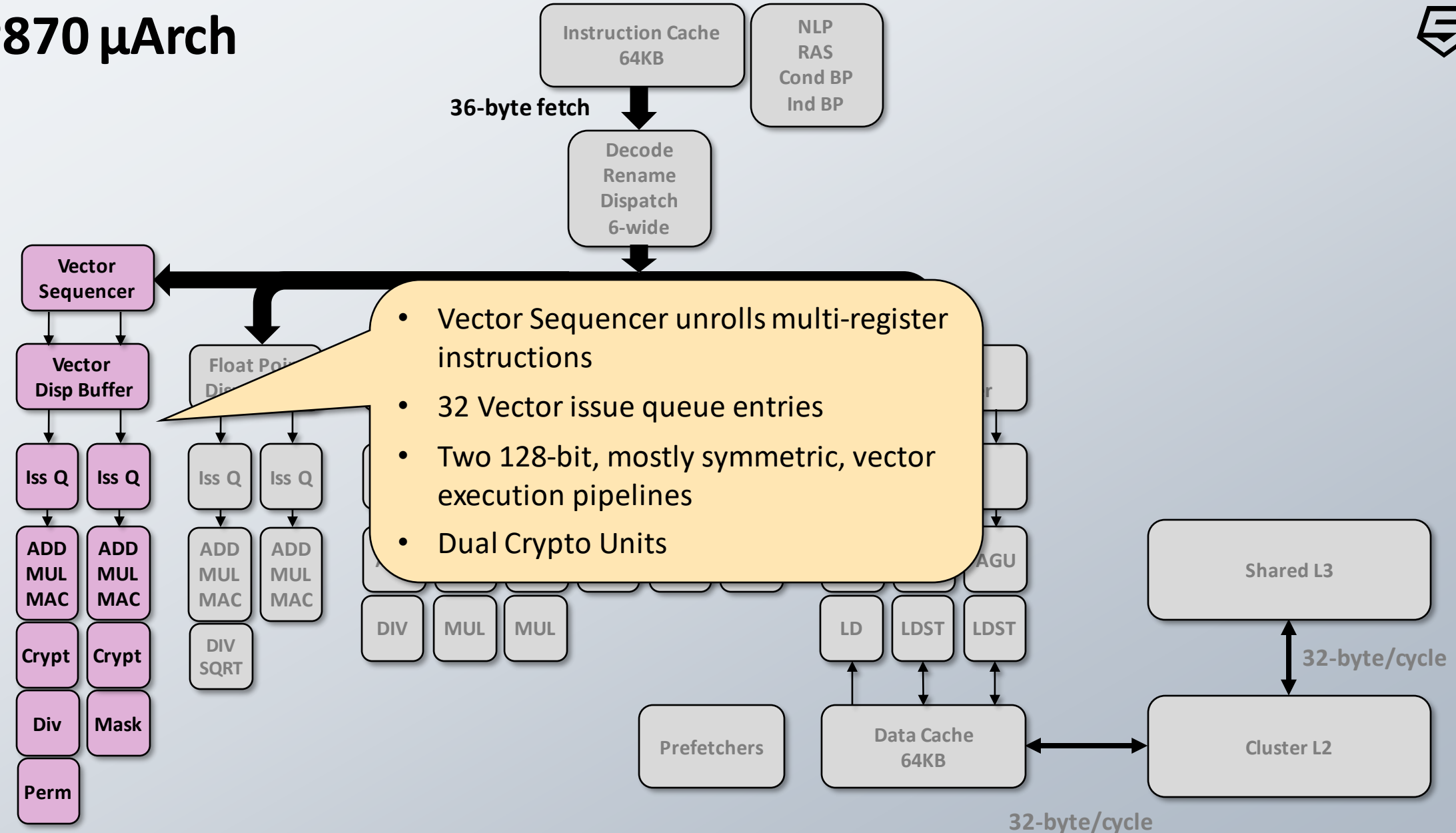


P870 µArch



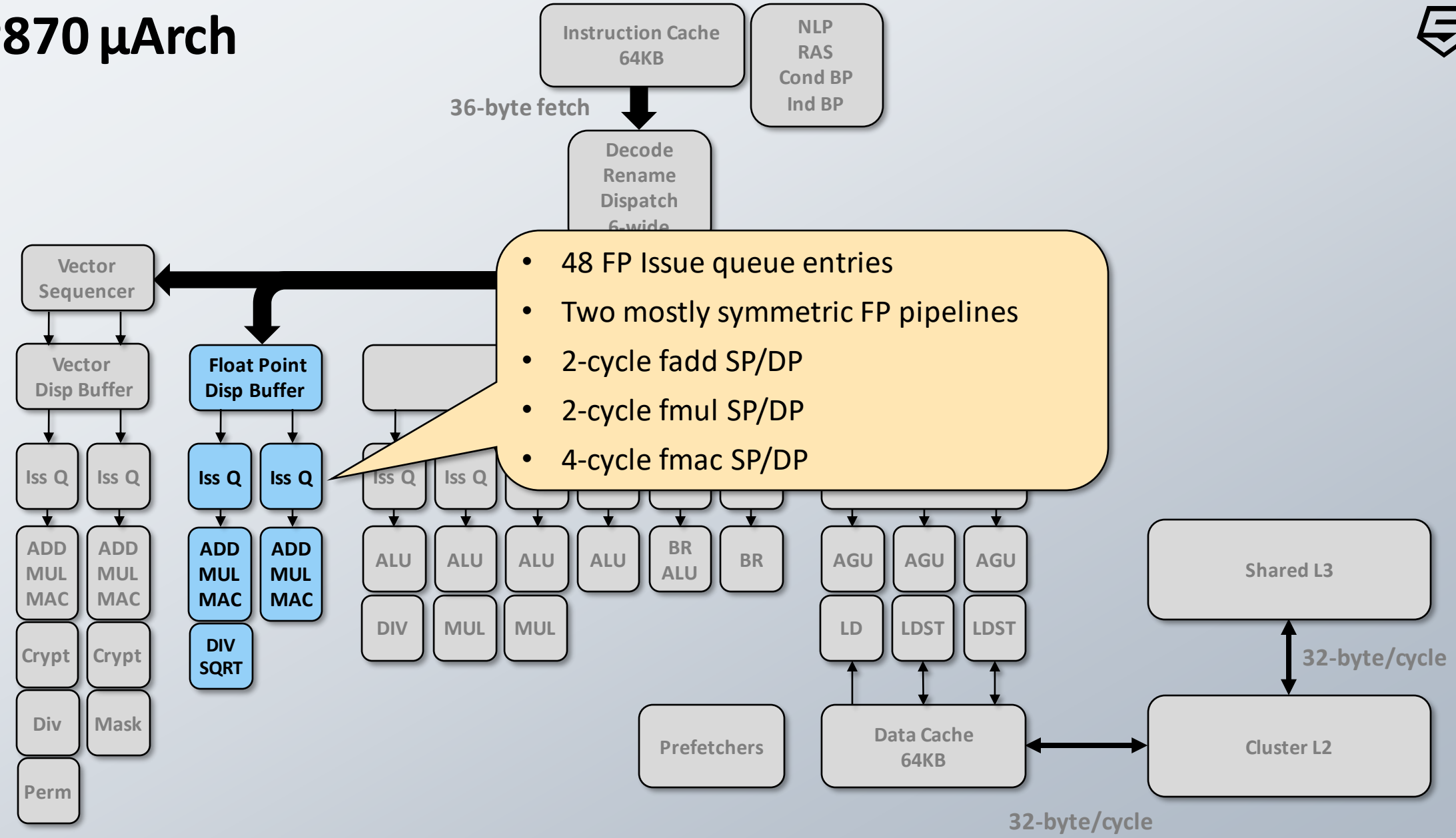
- 6-wide decode
- 32-bit and 16-bit instructions
- Register Renames:
  - 228 Integer
  - 240 Floating Point
  - 128 Vector
- ROB – up to 1120 instructions
- 6-wide dispatch

P870 µArch



- Vector Sequencer unrolls multi-register instructions
- 32 Vector issue queue entries
- Two 128-bit, mostly symmetric, vector execution pipelines
- Dual Crypto Units

P870 µArch



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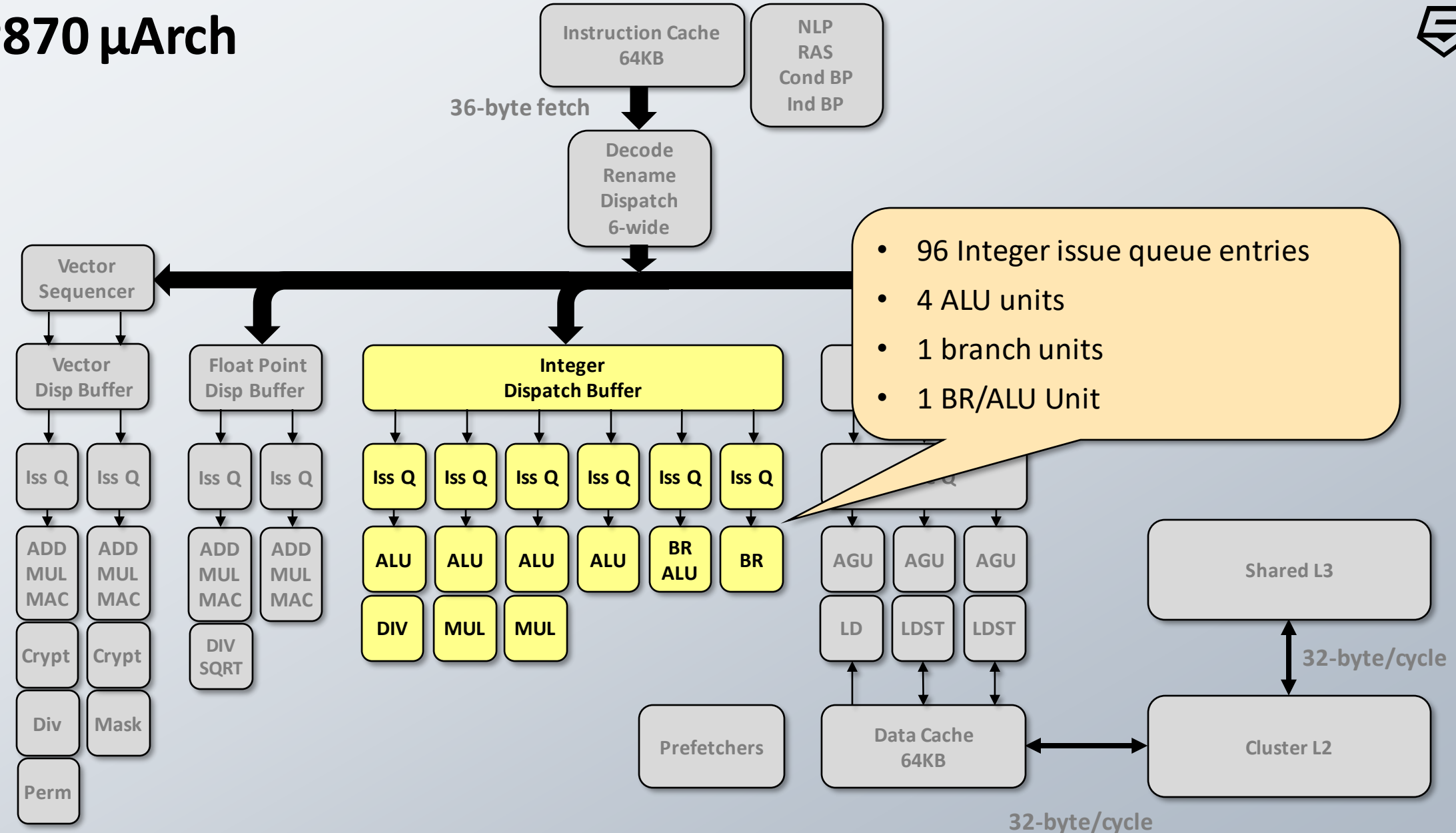

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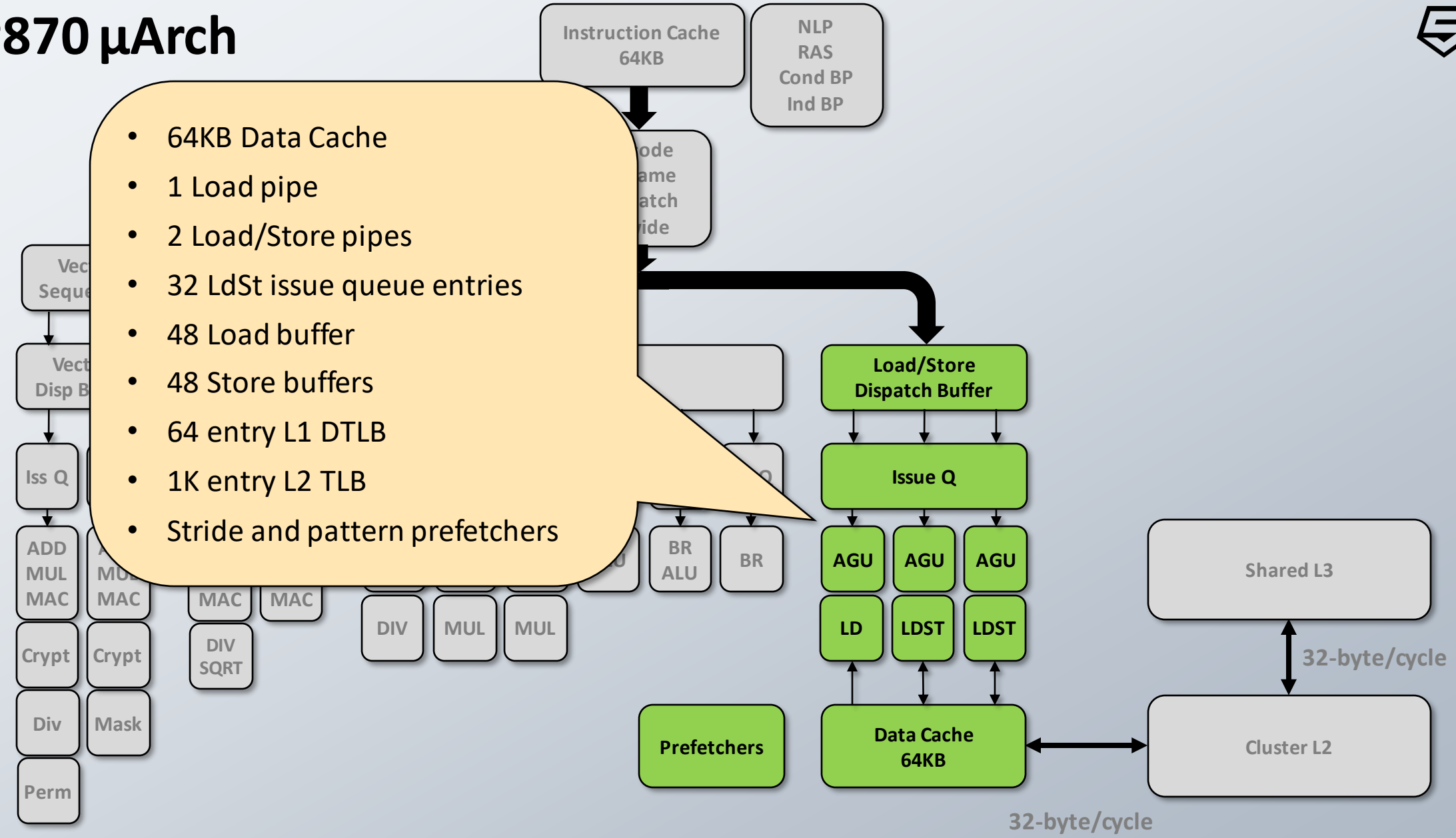
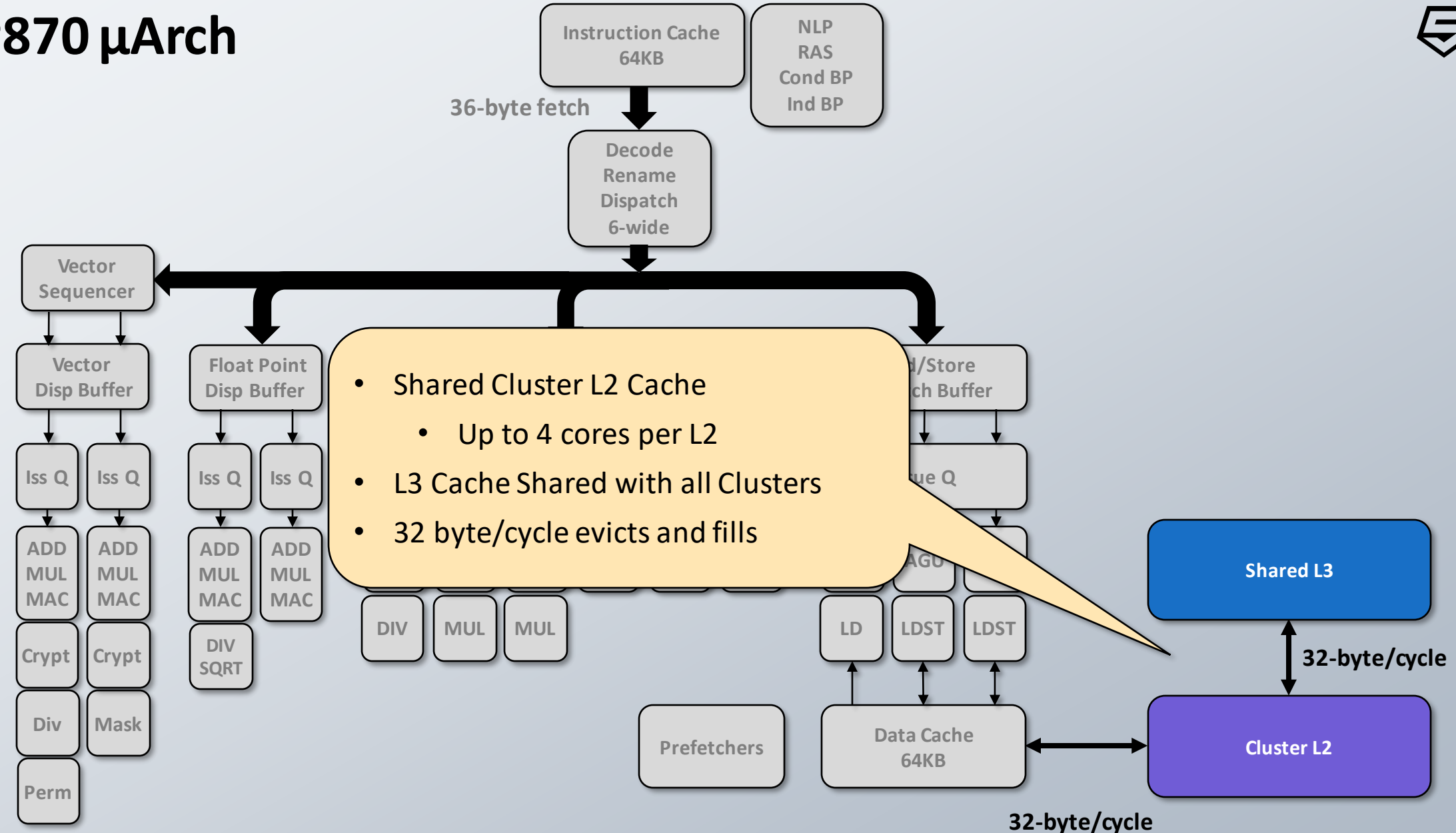
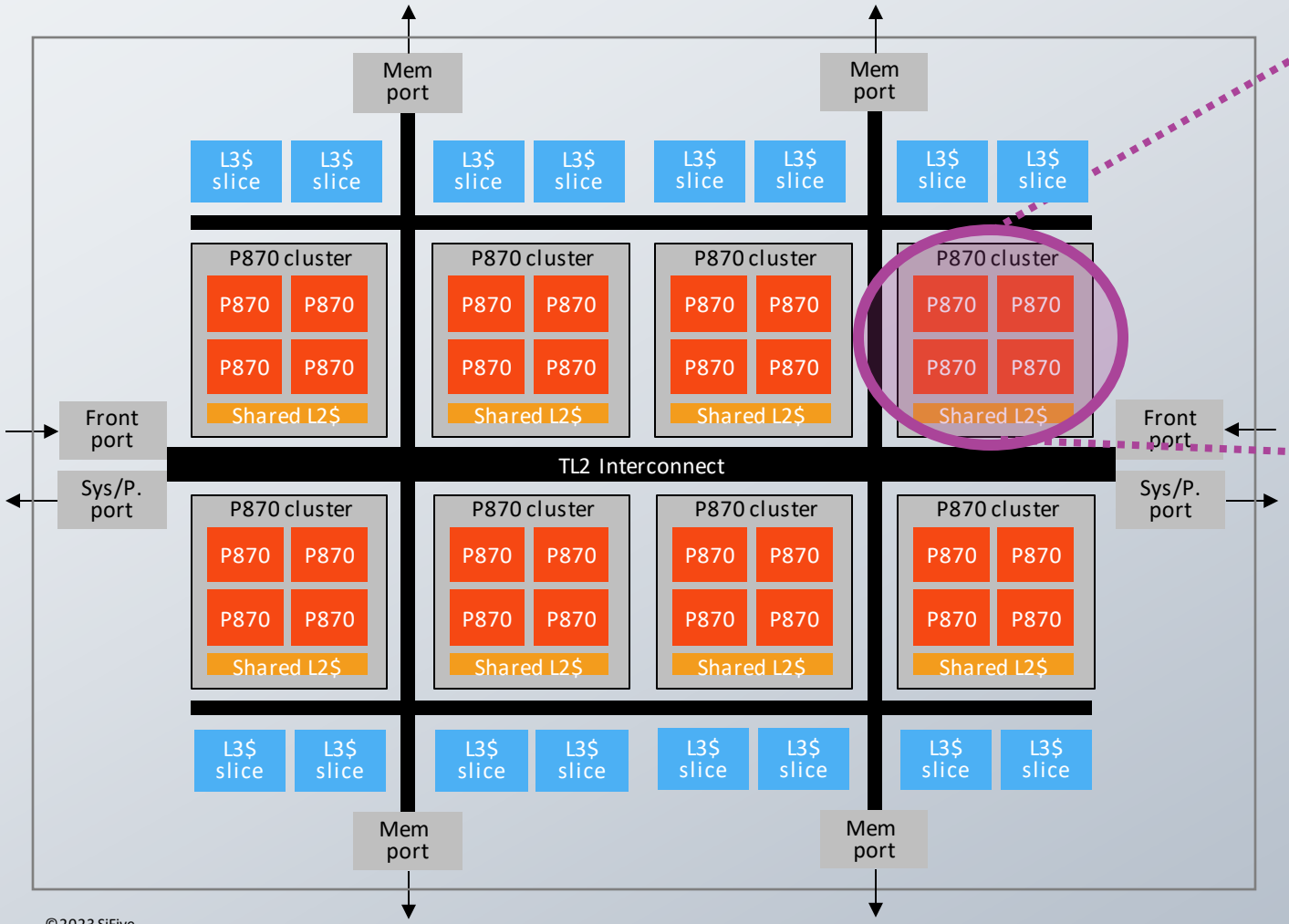


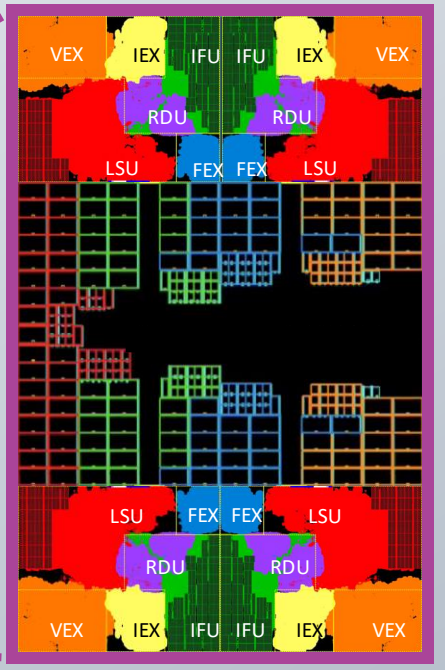
- 64KB Data Cache
- 1 Load pipe
- 2 Load/Store pipes
- 32 LdSt issue queue entries
- 48 Load buffer
- 48 Store buffers
- 64 entry L1 DTLB
- 1K entry L2 TLB
- Stride and pattern prefetchers

P870 µArch



Cluster topology with shared L2 cache and distributed L3 cache





P870 4-core cluster

Legend:

LSU - Load/Store Unit

IEX - Integer Execution Unit

FEX - Floating Point Execution Unit

VEX - Vector Execution Unit

IFU - Instruction Fetch Unit

RDU - Rename/Dispatch Unit

P870 Consumer example platform

SiFive Advanced Debug & Interrupt

Interrupt Controller

Debug & Trace

SiFive CPU Clusters

Performance cluster

P870

P870

Shared L2$

High-efficiency cluster

P470

P470

P470

P470

Shared L2$

Always-On cluster

E6

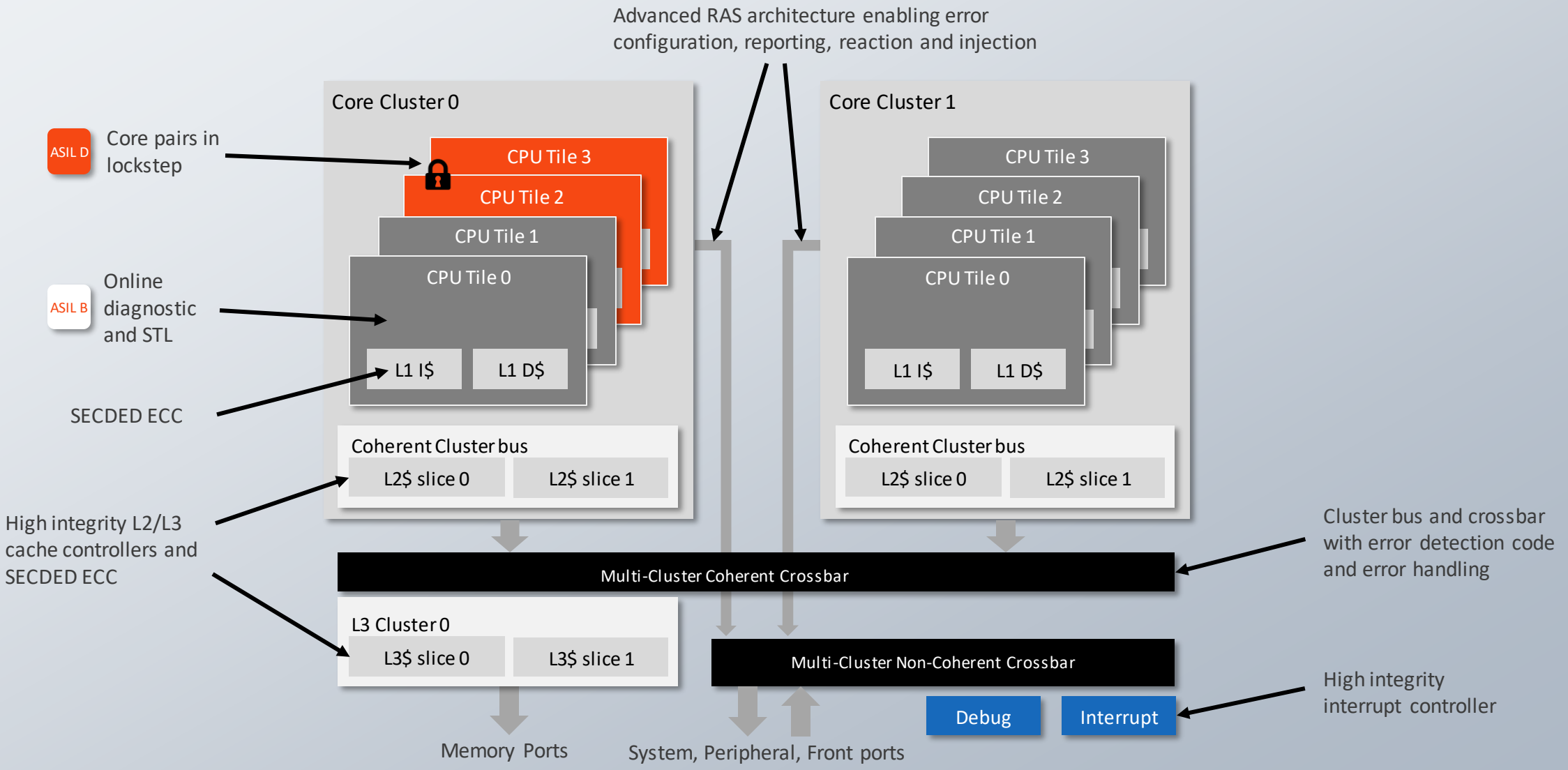
Shared L3$

SiFive System IPs

IOMMU

WorldGuard gadgets

P870-A Functional safety features



SiFive broad IP portfolio

Scalable from MCU to high-performance compute

64-bit
high-performance
feature-rich
OS capable
application processors

32/64-bit
real-time scalable
performance
deeply
embedded
processors

Automotive

P870-A
6-wide OoO core
128b vector length
Hypervisor extension
Vector crypto
IOMMU & AIA
WorldGuard
Shared cluster cache
RVA23
ASIL B, D

S7-A
64-bit, high performance embedded ASIL D

E6-A
32-bit, balanced performance and efficiency ASIL B, D

Intelligence

X200-Series
AI processor for Edge and Data Center ML applications
AI acceleration instructions
512b vector length

Performance

P500-Series
>8.6 Specint 2k6/GHz
3-wide OoO core
RVA20+

P400-Series
>8.6 Specint 2k6/GHz
3-wide OoO core
128b vector length
Hypervisor extension
Vector crypto
IOMMU & AIA
WorldGuard
RVA22

P600-Series
>13.1 SpecINT 2k6/GHz
4-wide OoO core
128b vector length
Hypervisor extension
Vector crypto
IOMMU & AIA
WorldGuard
RVA22

P800-Series
>18 Specint 2k6/GHz
6-wide OoO core
128b vector length
Hypervisor extension
Vector crypto
IOMMU & AIA
WorldGuard
Shared cluster cache
RVA23

Essential

U6-Series
64-bit, high performance

U7-Series
64-bit, superscalar performance

S2-Series
64-bit, Area optimized

S6-Series
64-bit, power efficiency

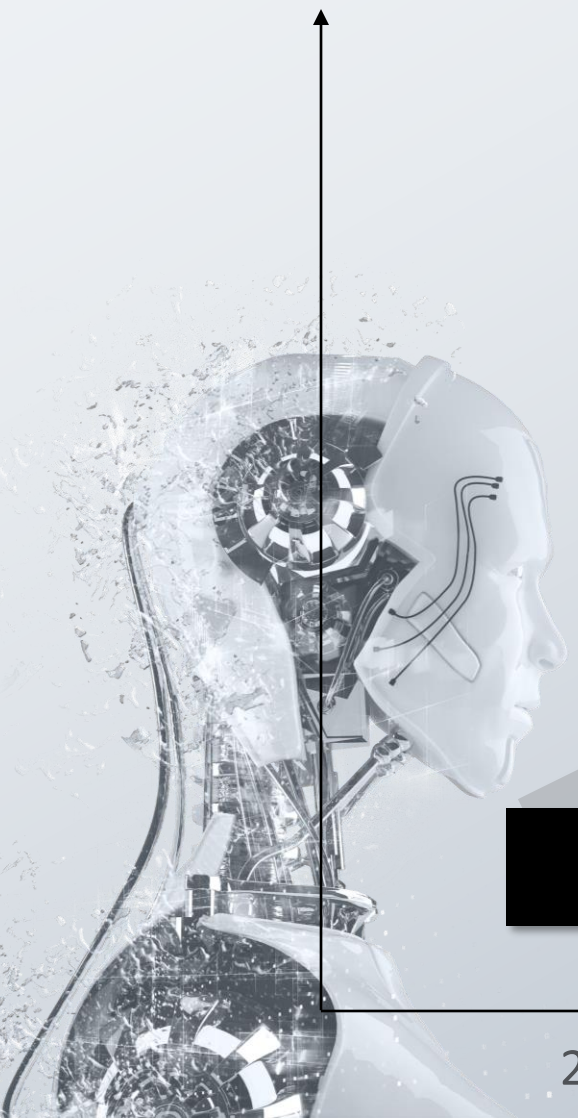
S7-Series
64-bit, high performance, embedded

E2-Series
Smallest, most efficient

E6-Series
Balanced performance and efficiency

E7-Series
32-bit, optimized performance

SiFive Performance family relentless innovation



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Empowering innovators

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